SIS

Struck Innovative Systeme GmbH

Harksheider Str. 102A
D-22399 Hamburg

Tel.: ++49 (0) 40 608 730 5 0
Fax: ++49 (0) 40 608 730 520
WWW: http://www.struck.de

Fast single word readout with SIS3100 sequencer under control of the SIS9200 DSP

The SIS1100/3100 PCI to VME interface was developed in a co-operation between the ZEL department of the research center Jülich and SIS for high speed data acquisition in Particle Physics and related fields. The main focus was on high speed block transfer readout in BLT32, MBLT64 and 2eVME and results in readout speeds in excess of 80 Mbytes/s. It turns out however, that everyday use of VME is in many cases dominated by older slaves with single read/write access readout. Single access handling is fairly inefficient on single board computers as well as PCI-VME interfaces as substantial operating system overhead is involved. Minimum overhead VME single cycle readout can be implemented by means of the SIS9200 SHARC DSP option on the SIS3100 sequencer. Large blocks of data can be stored on the SDRAM option of the SIS3100 (64, 128, 256, or 512 MByte) in a multiple or ring buffer scheme and transferred to the PC asynchronously with a transfer rate of 90 MBytes/s.

A 4 channel delay line readout system on the base of a Highland V680 TDC (time to digital converter) is used as an example for the typical single read/write access readout scenario. The system was implemented on a PC, the DSP code is written in Assembly language and the loader file is downloaded to the DSP at start of data acquisition.

The scope screen shot below shows the VME write line during the repeated readout sequence from the Highland V680 TDC (which is triggered by a Highland V851 digital delay generator in the test case):

- Poll for hit in hit register(A16/D16 read)
- Set readout channel 0 (A16/D16write)
- Read time register 1 (A16/D16 read)
- Read time register 2 (A16/D16 read)
- Set readout channel 1 (A16/D16write)
- Read time register 1 (A16/D16 read)
- Read time register 2 (A16/D16 read)
- Set readout channel 2 (A16/D16write)
- Read time register 1 (A16/D16 read)
- Read time register 2 (A16/D16 read)
- Set readout channel 3 (A16/D16write)
- Read time register 1 (A16/D16 read)
- Read time register 2 (A16/D16 read)
- Rearm (A16/D16write)

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In parallel longwords are formed from time register 1 and 2 data and stored to the SDRAM of the SIS3100. The 2 to 3 shorter spikes (marked with arrows) between the 5 write blocks (with 2 interleaved reads each) stem from the read polling access to the hit register. The repetition rate for one cycle is less than 10 ?s (for 14 reads/writes including one polling cycle)