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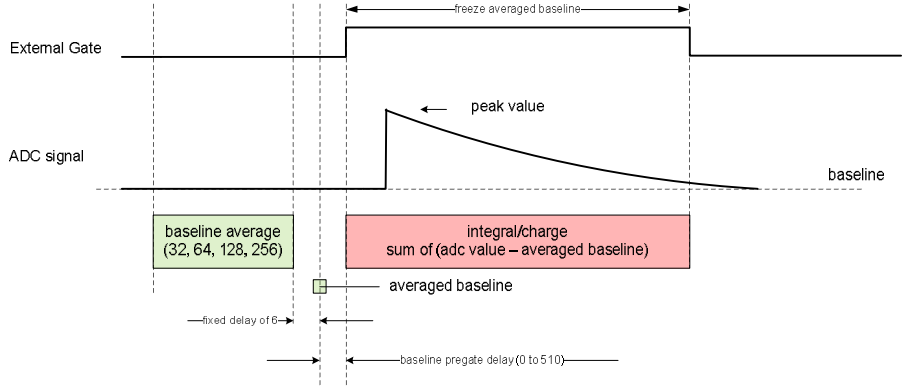
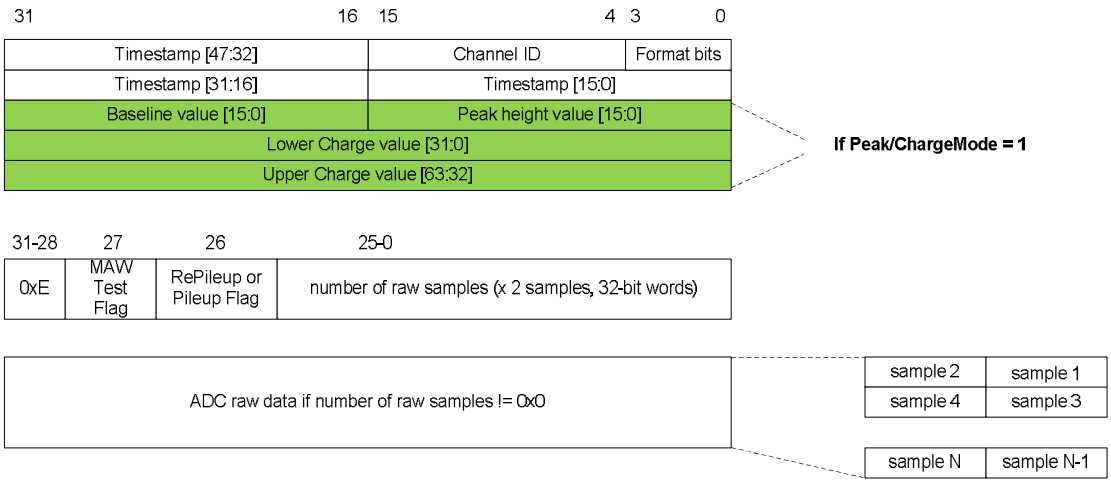
SIS3316 Peak and Charge ADC Mode of Operation

This mode is available starting with ADC firmware version 0x02500005.
An external gate (connected to front panel input TI) is used to define the area in which the signal maximum (peak height) and the charge are computed. The averaged baseline is subtracted in both cases. The baseline average can be 32, 64, 128 or 256 samples long (defined by the two baseline average mode bits) and the baseline pregate delay defines how many samples ahead of the leading edge of the gate the moving baseline average is frozen and stored to the event header. A fixed delay of 6 samples has to be taken into account as shown below.



SIS3316 Peak/Charge Data Format

The data format in peak/charge mode of operation is illustrated below. If you choose a non zero value for the number of raw samples you have the option to get raw data besides the peak height and the charge integral. This may be of particular interest for signal processing of the leading edge of the signal or to compare the computed/stored baseline value to the real situation at the beginning of the gate. The timestamp information is stored at the leading edge of the gate.



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EAR: WEEE-Reg.-No. DE18787647

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