




struck innovative
systeme

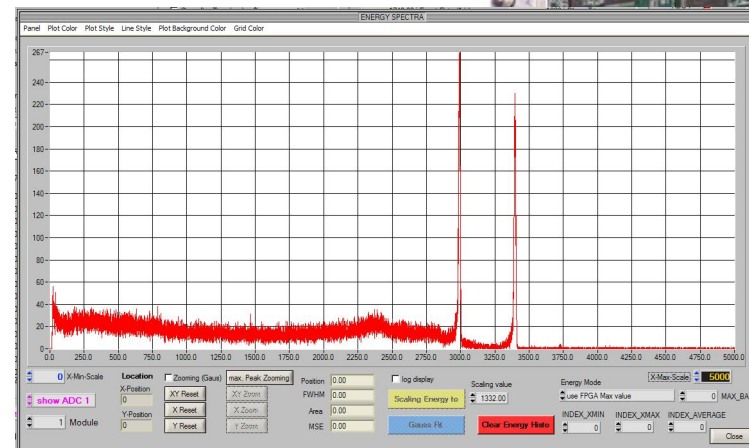
MTCA.4 Digitizer for RF (and other applications)



Dr.
Matthias
Kirsch

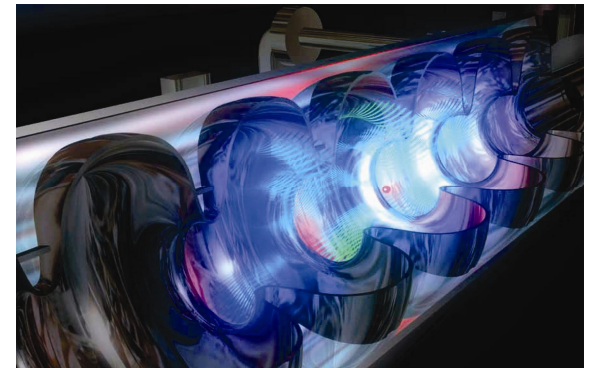
Where do we come from?

- SIS3302 100 MS/s 16-bit 8 channel VME digitizer
- Germanium and other detector readout applications
- at tiny thresholds VME cycles in parallel to acquisition may result in triggers
- ~ 100 MByte/s readout
- fixed front panel input



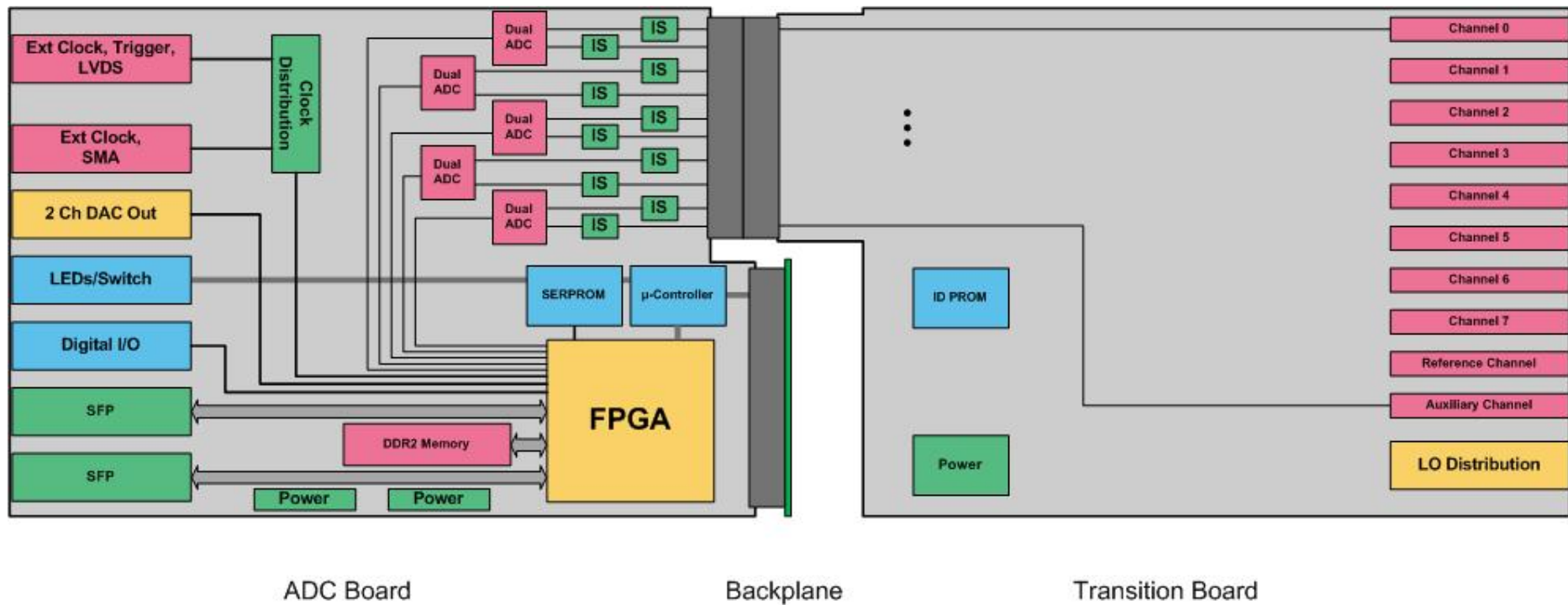
Where do we want to go?

- serial symmetric readout
- high throughput readout
- hot swap
- timing distribution over backplane
- high speed point to point links to adjacent slots and controller/concentrator
- use one fairly complex ADC/Digitizer design with application specific input cards



Approach

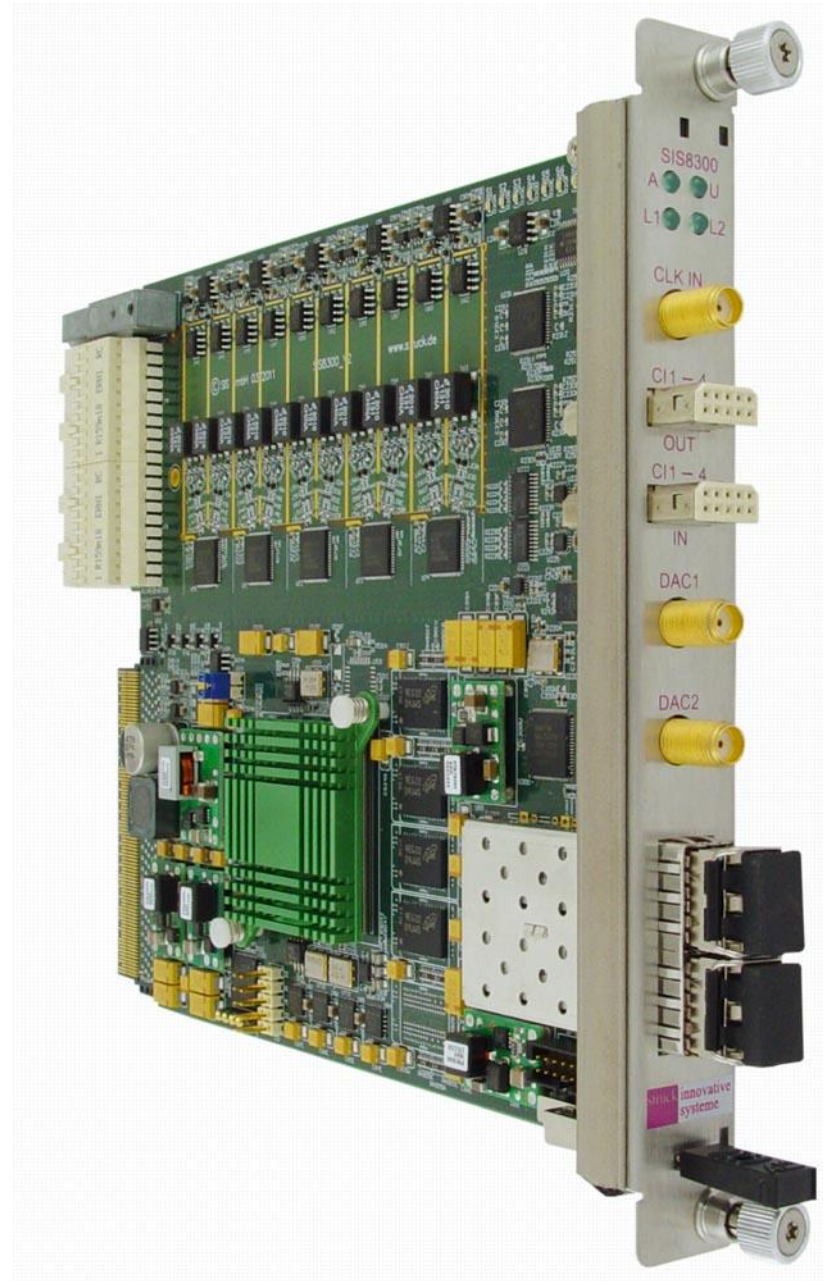
MTCA.4 Digitizer with RTM's



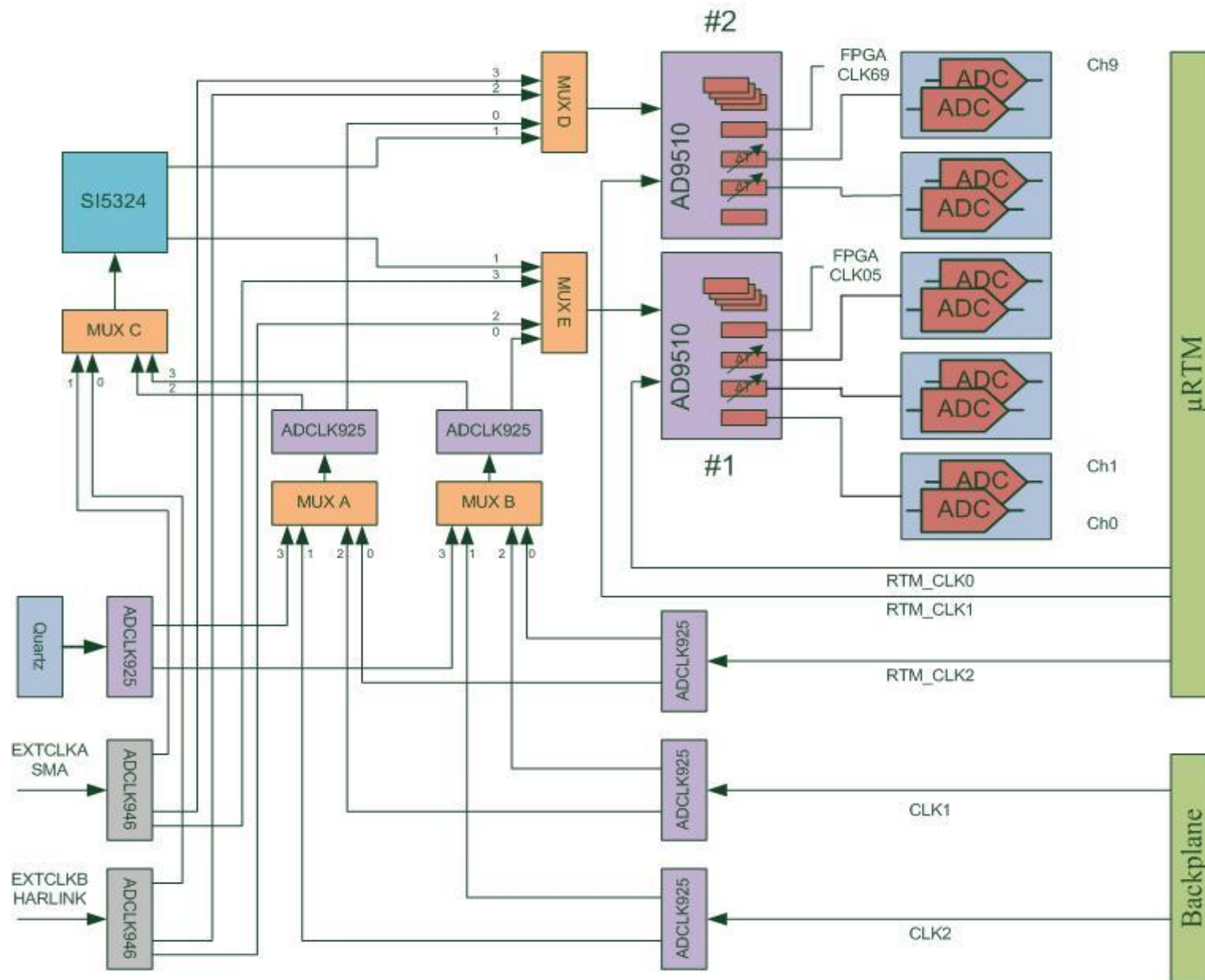
SIS8300 Digitizer Properties

- MTCA.4
- 4 lane PCI Express → 640 MB/s readout
- 10 channels 125 MS/s 16-bit ADC
- 10 MS/s to 125 MS/s per channel
- AC and DC input stage
- two 250 MS/s 16-bit DACs for fast feedback implementation
- high precision, flexible clock distribution logic
- Internal, front panel, RTM and backplane clock sources
- Programmable delay of twin ADC groups
- Gigabit Link Port implementation to backplane
- Double SFP cage for high speed system interconnects
- Virtex V FPGA
- up to 32 MSample Memory per channel
- additional point to point links over backplane
- In field firmware upgrade

SIS8300 V2



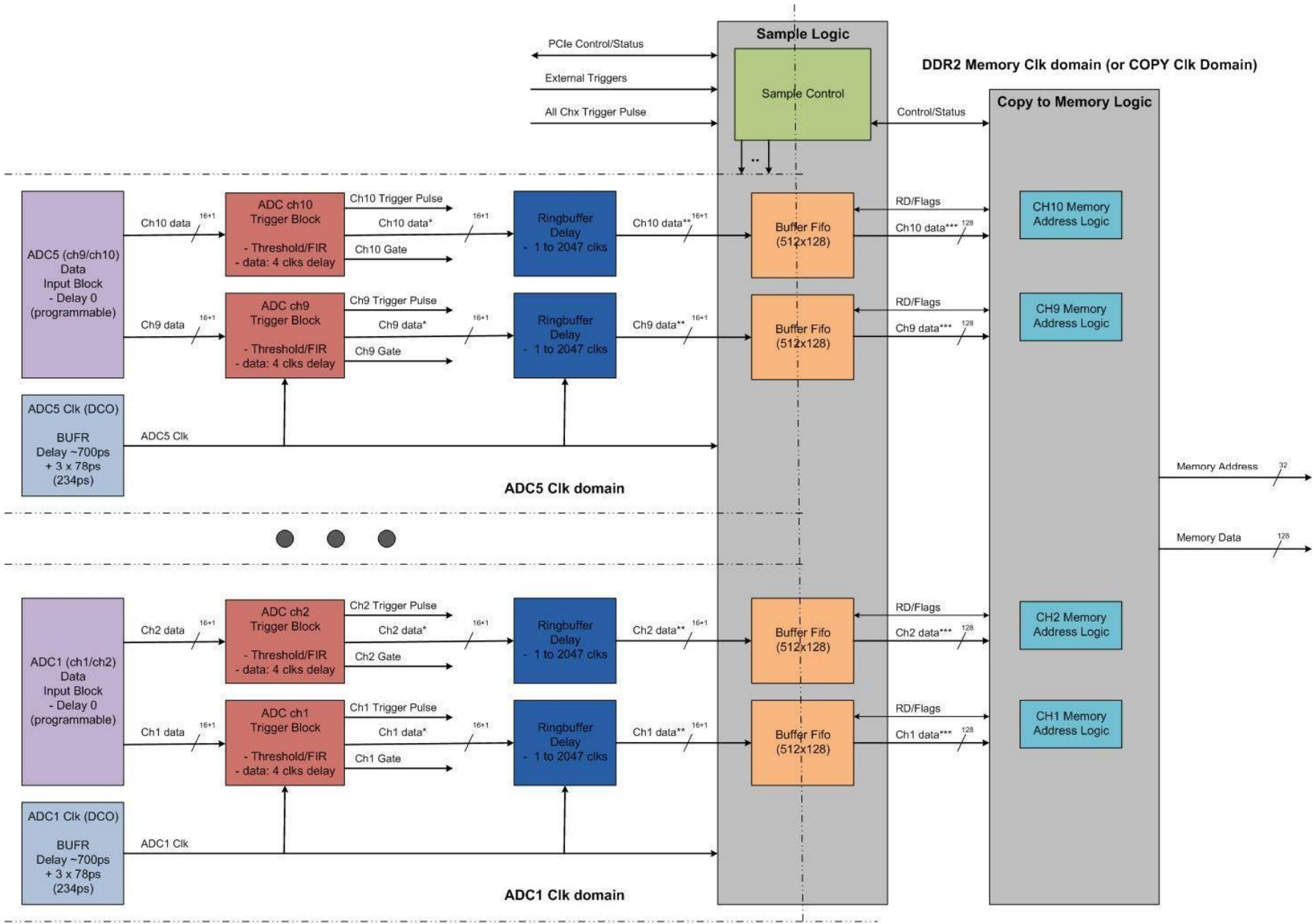
SIS8300 Clock Distribution



SIS8300 Virtex 5 Options

FPGA	DDR2 Memory	Comment
XC5VLX50T-3FGG1136C	4 x 1 GBit	Default
XC5VSX50T-3FGG1136C	4 x 2 GBit	More DSP slices
XC5VLX110T-3FGG1136C	5 x 2 GBit	More I/Os

SIS8300 Generic Sample Logic



Modularity of Firmware

```
...  
-- Module Name:      sis8300_top - Behavioral  
...  
  
entity sis8300_top is  
  generic(  
    RESERVED_REGISTERS_FEEDBACK_EN      : integer := 0 ;  
    TRIGGER_BLOCK_EN                    : integer := 1 ;  
    RINGBUFFER_DELAY_EN                 : integer := 1 ;  
    SAMPLE_ADC_TWO_CH_BLOCK_EN          : integer := 0 ;  
    DUAL_OPTICAL_INTERFACE_EN           : integer := 1 ;  
    DUAL_PORT12_13_INTERFACE_EN         : integer := 0 ;  
    DUAL_PORT14_15_INTERFACE_EN         : integer := 0  
  );  
  
...
```

MMC (Module Management Controller) Implementation in ATMEGA128

Struck in house development

RTM implementation in close co-operation
with DESY and N.A.T

ongoing Vadatech MCH debugging

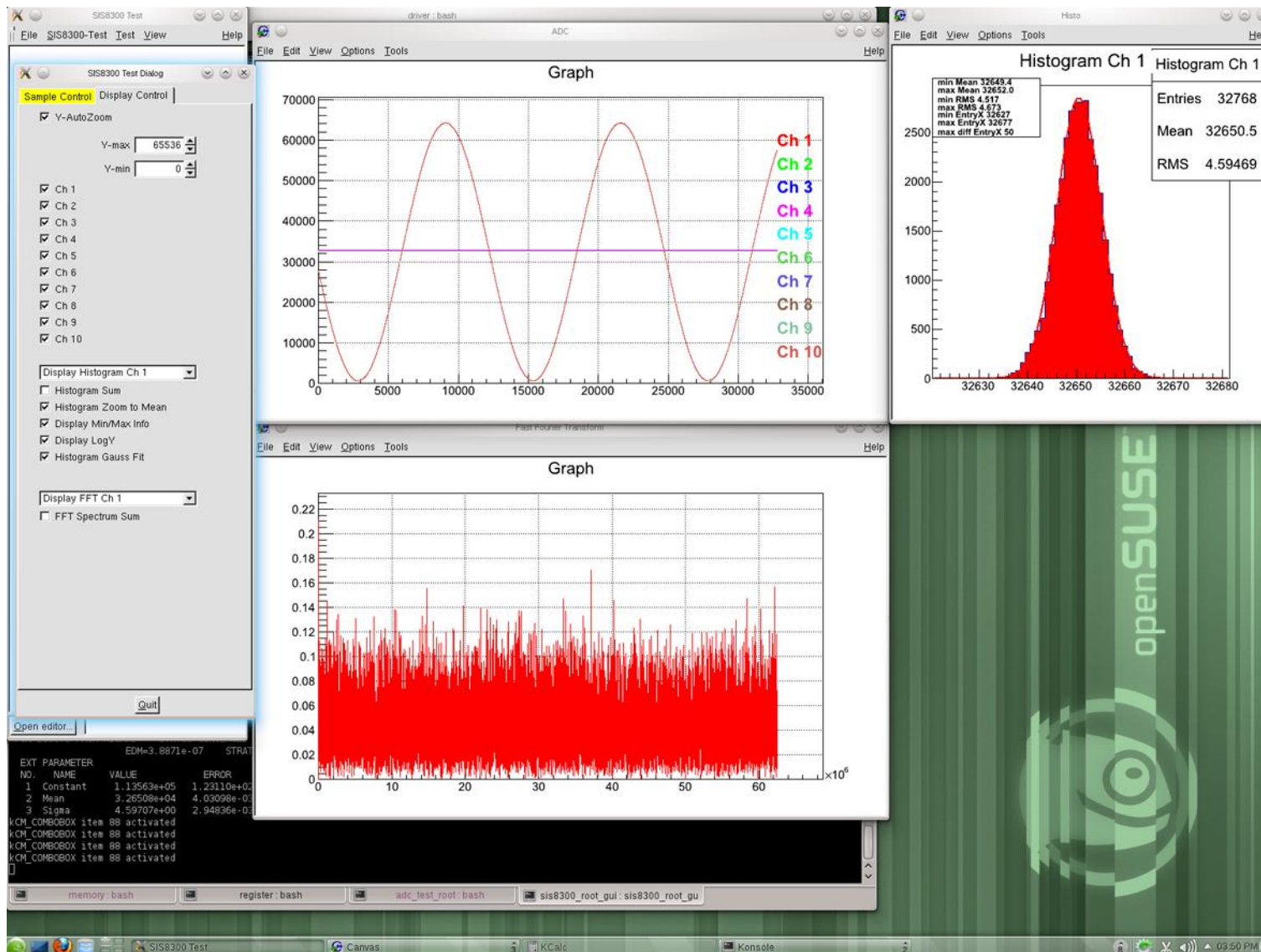
ATmega1281-16MU



Software for Generic FW

- LINUX driver
- 320 MByte/s to user space (farther optimization option)
- ROOT based ready to run GUI
- Windows Beta driver

SIS8300 Generic/LINUX Root

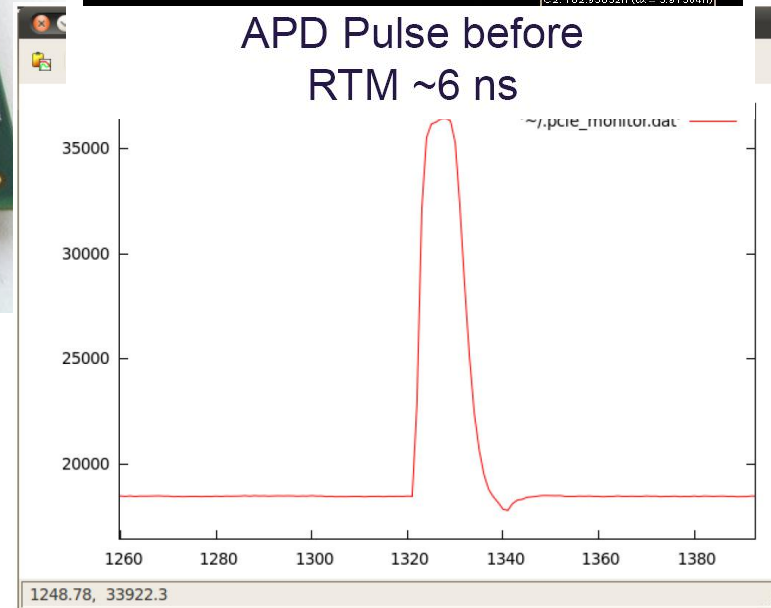
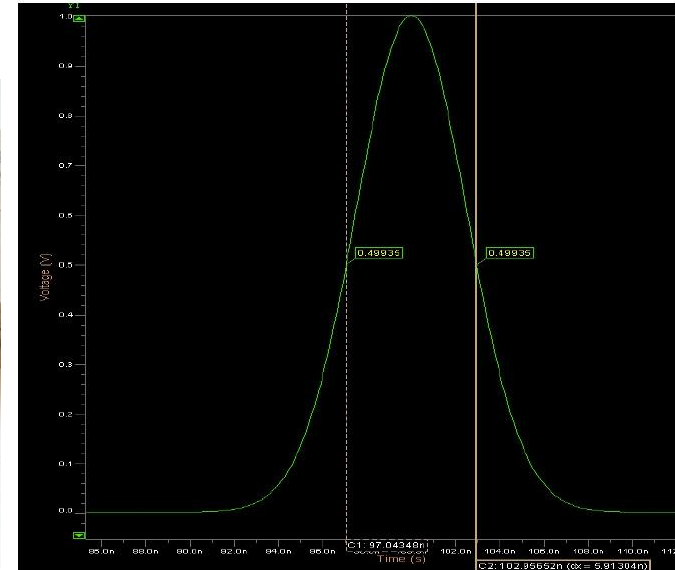


DESY APD Stretcher RTM

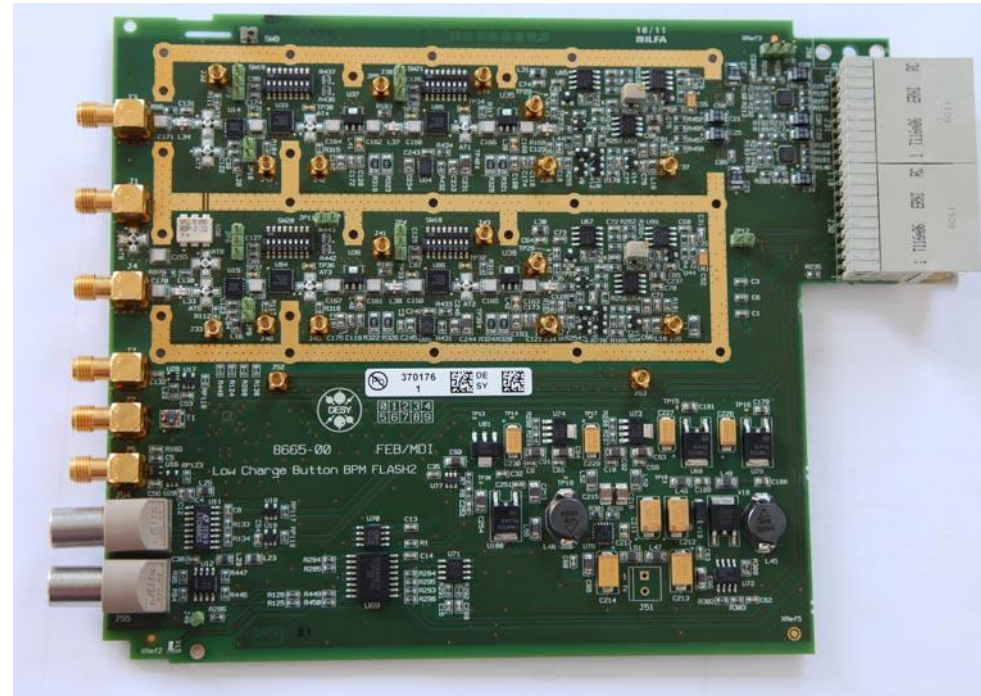


Dual channel signal stretcher

Petter Göttlicher, Chris Youngman

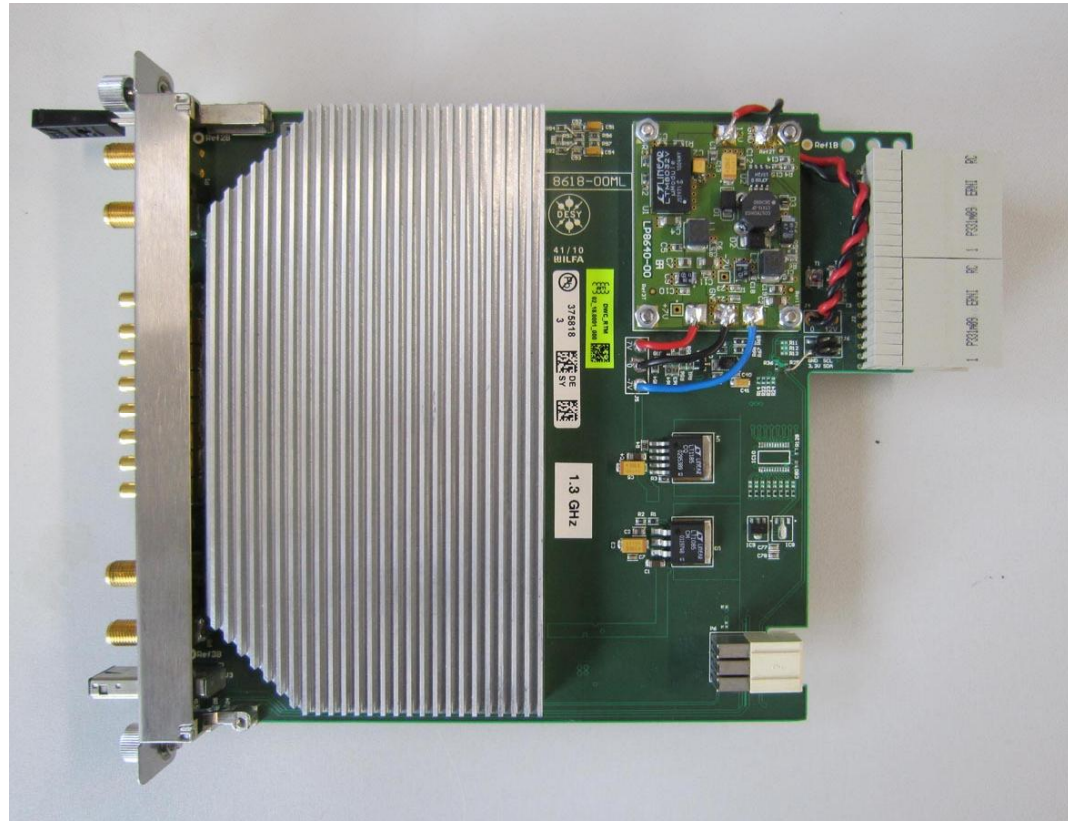


DESY BPM RTM



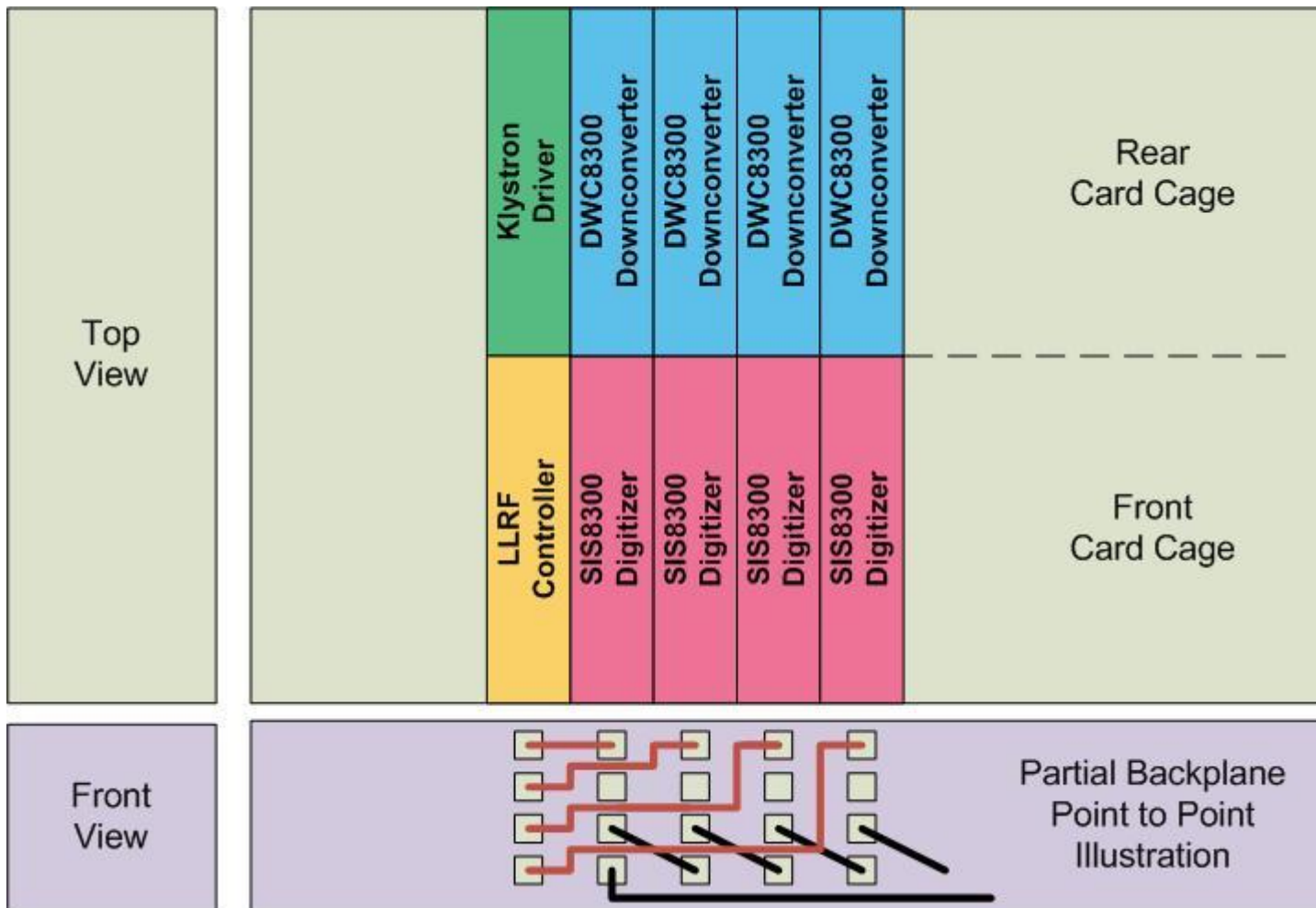
Interleaved Sampling
50 pC resolution target
Frank Schmidt-Föhre, Bastian Lorbeer

DESY DWC8300 Downconverter RTM



1.3 GHz,...,4 GHz
Frank Ludwig

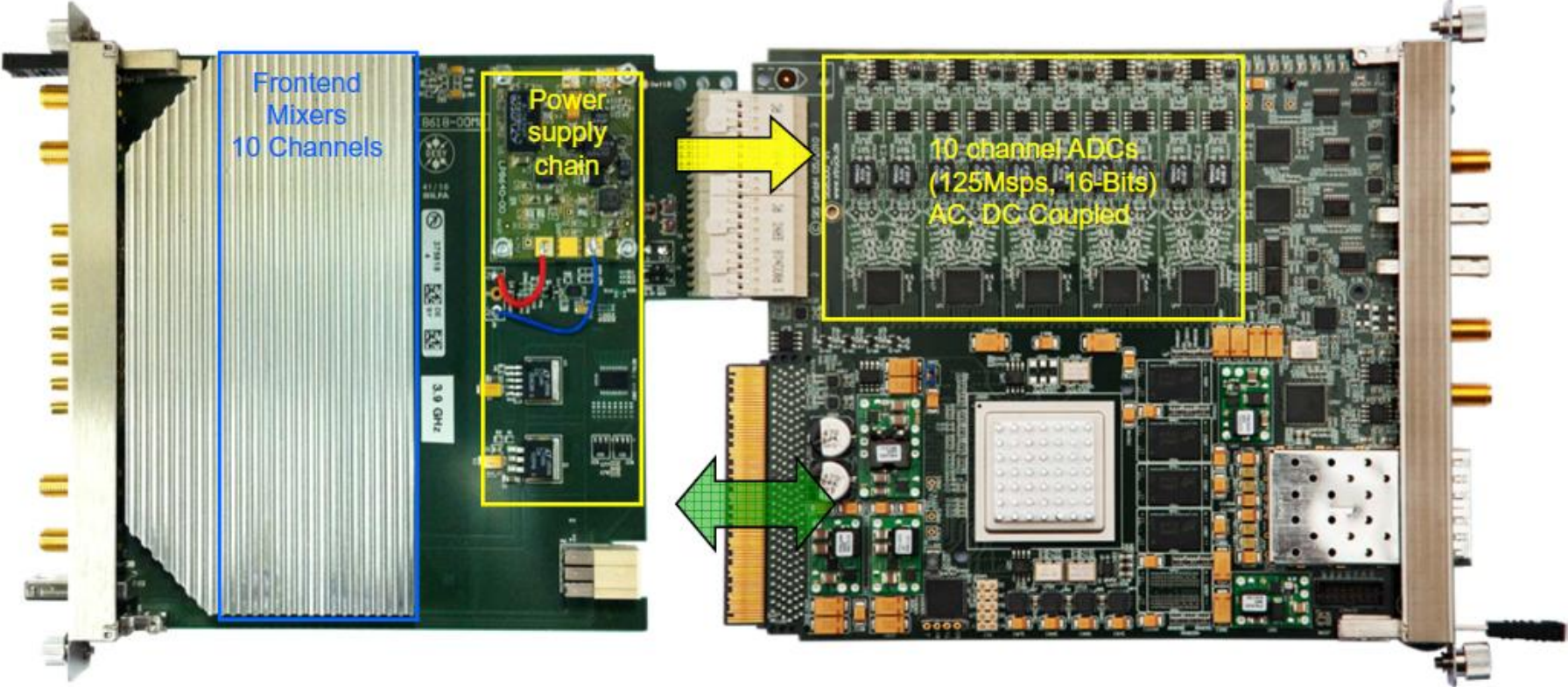
LLRF “Cluster”



DWC8300/SIS8300

■ 10-channel Down-Converter

■ Digitizer, Partial Vector Sum



- 10 channel field detection (1.3GHz, 3.0GHz, 3.9GHz)

- 10 channel ADCs (125Mps, 16-Bits)
- FPGA partial cavity vector sum
- Low latency links via uTCA-backplane

Klystron Driver/LLRF Controller

■ Klystron Driver



- 2 channel vector modulator (108MHz, 216MHz, 1.3GHz...3.9GHz)
- 16-bit DAC

■ LLRF Controller



- LLRF Controller, 6 Fiber-Ports, 2 GB-Links
- FPGA(V5), DSP

Flash Injector Rack Installation

■ uTCA Prototype Front view

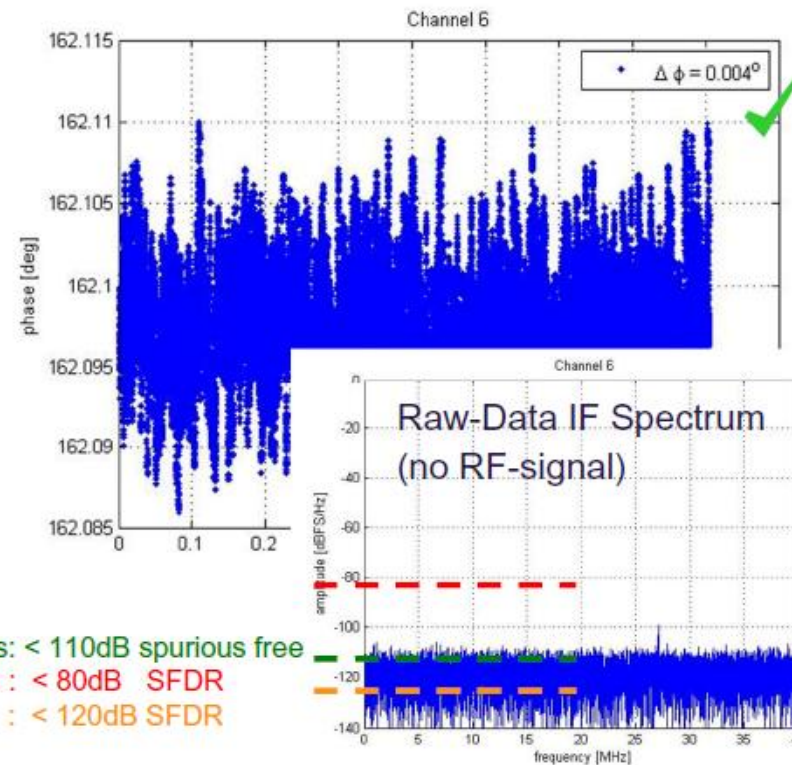
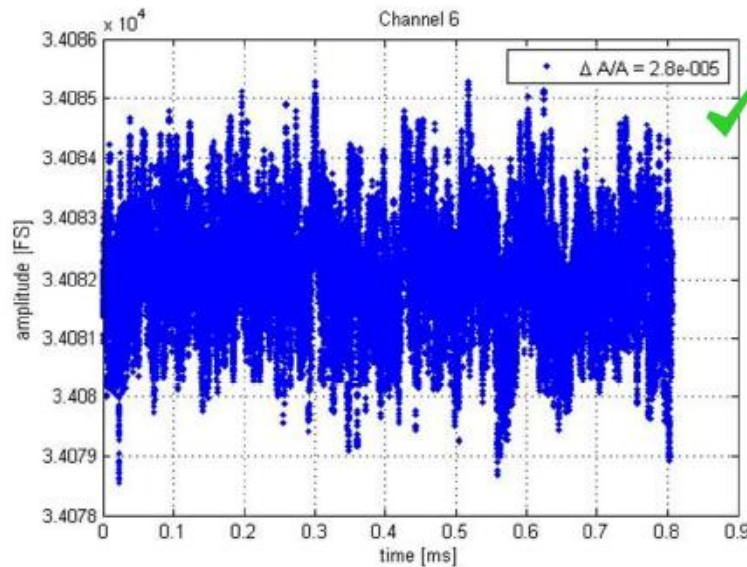


■ uTCA Prototype Rear view



Lab Test

■ Short-term stability in a uTCA crate (laboratory) :



Testconfiguration:

- DWC8300 R1.0, SIS8300_V2, MCH, CPU, uTCA crate
- DRO 1.3GHz (PSI), 1354 MHz LO, 54MHz IF, 81MHz SR
- LO-Generation Module (19", FL, PM version)
- Offline Matlab non-iq analysis (N=65K), 1MHz Bandwidth

Power-Entry-Modules: < 110dB spurious free
 Poor Power Supplies : < 80dB SFDR
 VS-Scaling : < 120dB SFDR

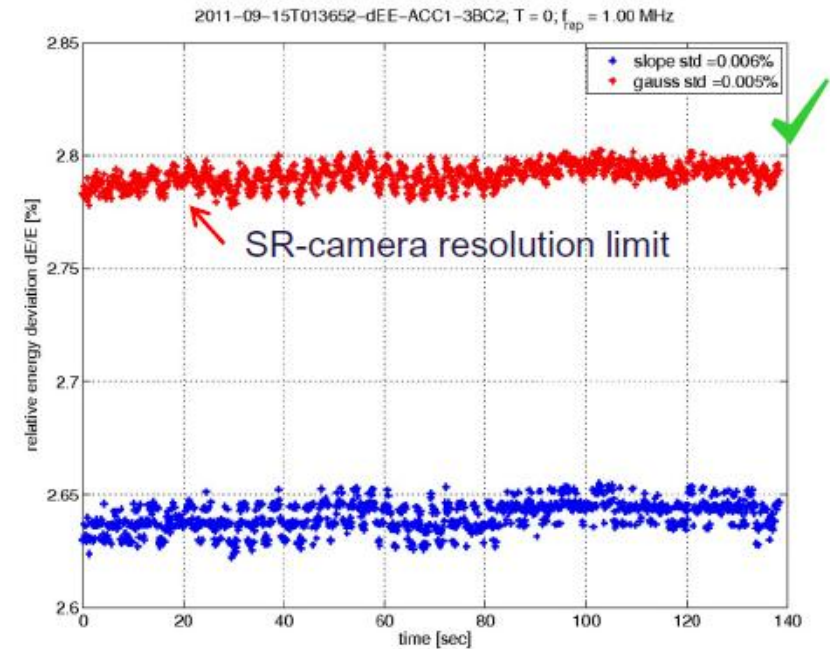
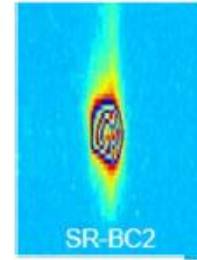
- ➔ Single cavity resolution improved by a factor of 5 to $dA/A=2.8E-5$.
- ➔ Signal integrity in uTCA crate achieved Eval board performance.
 (using a Power-Entry-Module, Ericsson BMR911483)

FLASH Operation

FLASH operation :



On-crest energy stability :



→ Energy stability $dE/E=0.5E-4$.

Summary I

- SIS8300/DWC8300 MTCA.4 Digitizer-Downconverter combination meets XFEL LLRF specification
- BPM and APD stretcher RTMs

Summary II

- SIS8900 single ended generic RTM

To do:

- Port SIS3302 VME digitizer Ge/Gamma firmware to SIS8300/8900 for 1:1 trigger/noise comparison

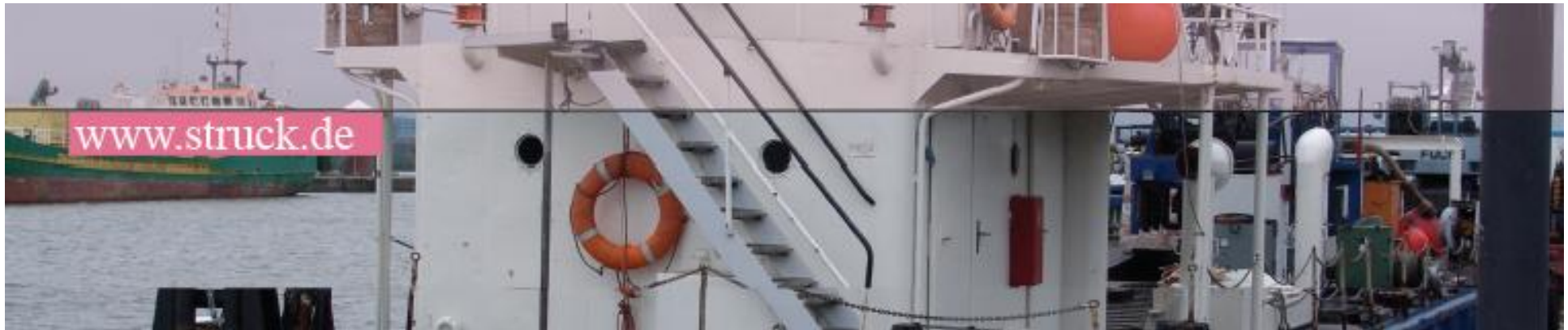
Deployment into other applications

- Positioning Interferometer readout
- Neutron scattering/delay line application

μ TCA/MTCA.4 Ecosystem

- good feedback during ICALEPCS
- user base increasing
- availability of standard hardware increasing

One will want to keep in mind that a learning and introduction curve was present in other standards -like VME- as well



Acknowledgements

The SIS8300 was developed in co-operation with DESY under ZIM Förderkennzeichen 2460101MS9

We'd like to extend our special thanks to Kay Rehlich from DESY for the good atmosphere and the assistance throughout the development and Frank Ludwig from DESY for his input and continued support for improvements on the analog side in the V1 to V2 revision transition and beyond.



Questions/Discussion

