MTCA.4 RTMs for Generic Fast ADC-DAC

Dr. Matthias Kirsch

“A good speech should be like a woman's skirt: long enough to cover the subject and short enough to create interest”

Winston S. Churchill

Nomenclature

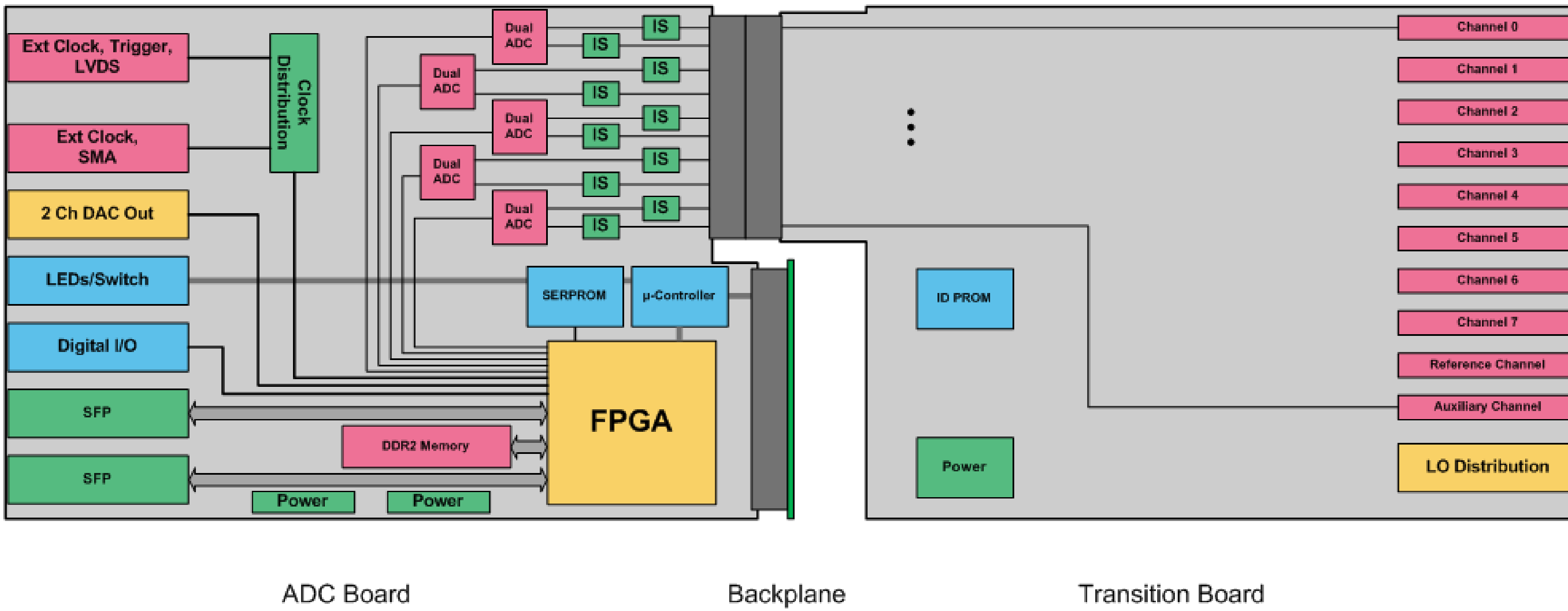
µRTM or RTM

Rear Transition Module

in the context of the MTCA.4 standard

(in contrast to ATCA Rear Transition Module)

AMC/µRTM Concept



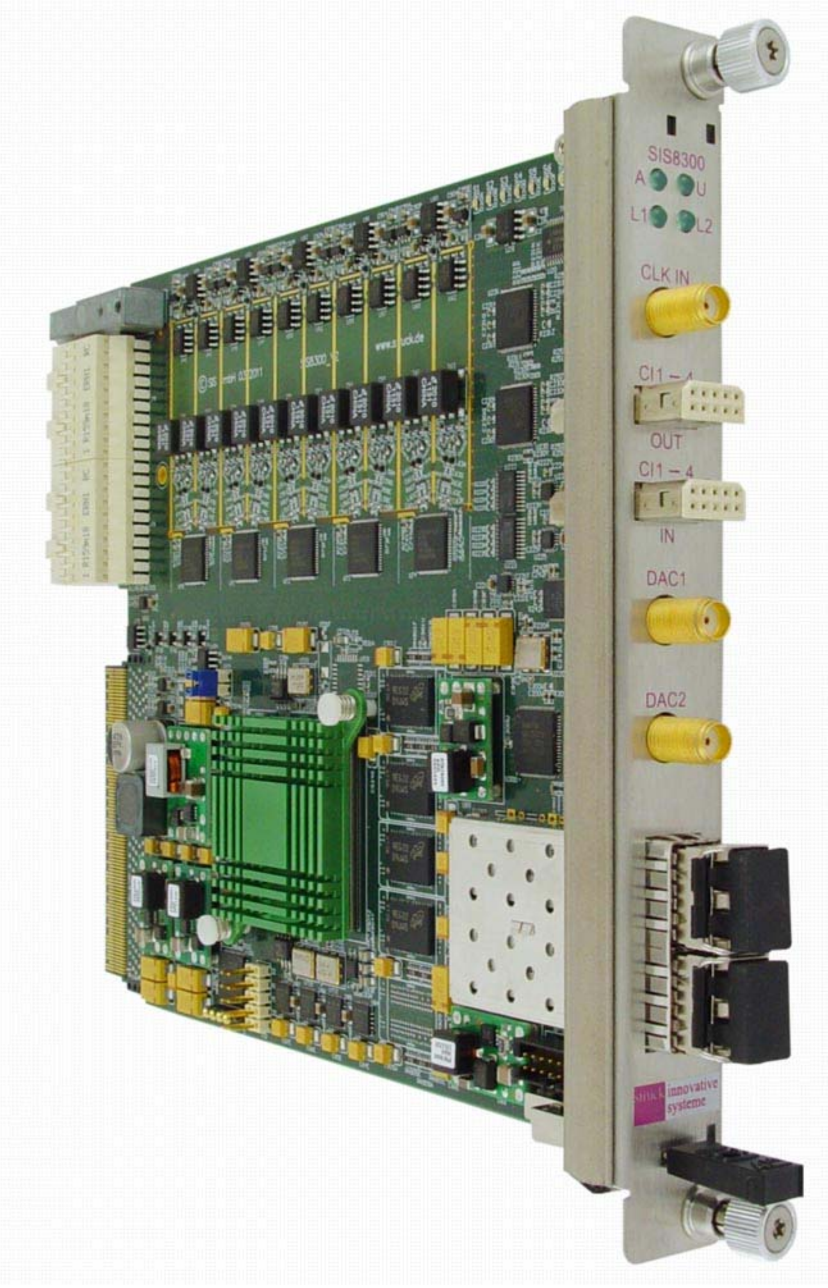
Underlying Idea

- Develop fairly complex Digitizer or FPGA,… AMC.4 card once
- Use with a variety of RTMs with moderate complexity tailored to the application

SIS8300 Digitizer Properties

- MTCA.4
- 4 lane PCI Express → 640 MB/s readout
- 10 channels 125 MS/s 16-bit ADC
- 10 MS/s to 125 MS/s per channel
- AC and DC input stage
- two 250 MS/s 16-bit DACs for fast feedback implementation
- high precision, flexible clock distribution logic
- Internal, front panel, RTM and backplane clock sources
- Programmable delay of twin ADC groups
- Gigabit Link Port implementation to backplane
- Double SFP cage for high speed system interconnects
- Virtex V FPGA
- up to 32 MSample Memory per channel
- additional point to point links over backplane
- In field firmware upgrade

SIS8300 V2



SIS8300 Virtex 5 Options

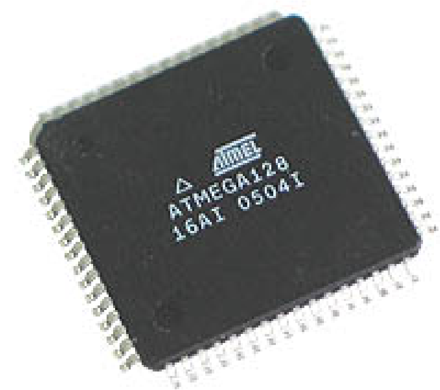
FPGA	DDR2 Memory	Comment
XC5VLX50T-3FGG1136C	4 x 1 GBit	Default
XC5VSX50T-3FGG1136C	4 x 2 GBit	More DSP slices
XC5VLX110T-3FGG1136C	5 x 2 GBit	More I/Os

MMC (Module Management Controller) Implementation in ATMEGA128

Struck in house development

RTM implementation in close co-operation
with DESY and N.A.T
(for insiders: Quiesce philosophy to be sorted out)

ATmega1281-16MU



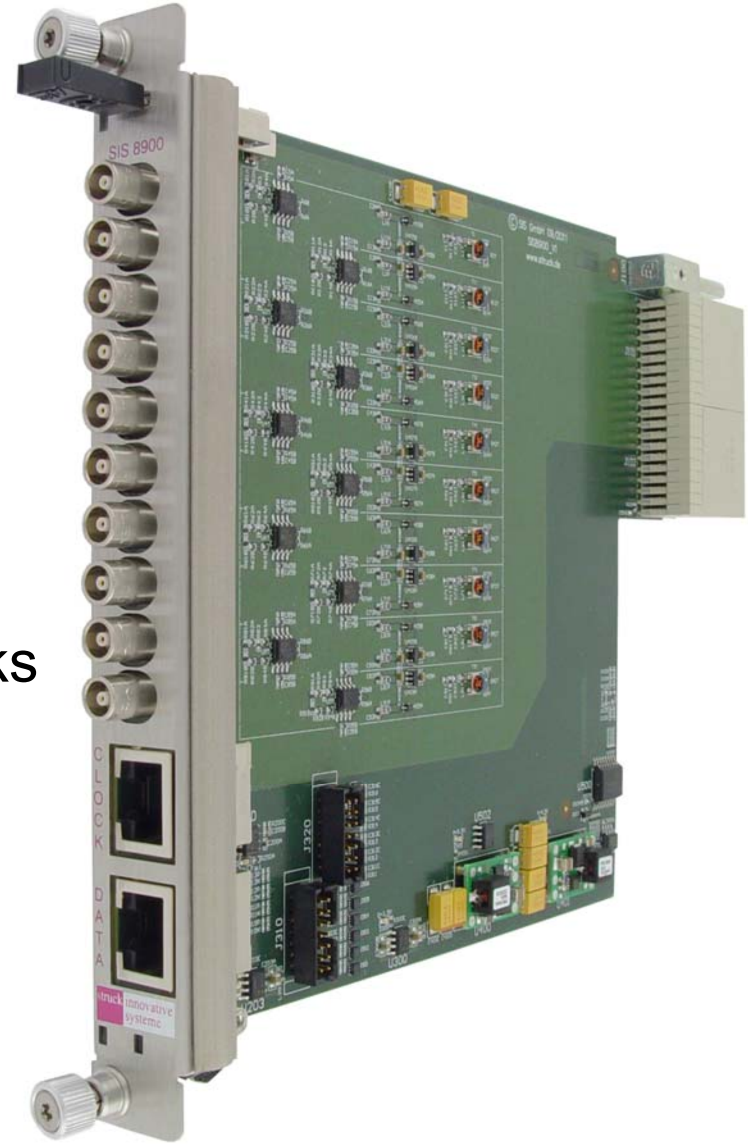
RTMs for the SIS8300

Name	Source	Description
SIS8900	Struck	Single Ended Input Card
RTM7201	HYTEC	4-channel Signal Modulator
DWC8300	DESY	Downconverter
BPM	DESY	Interleaved Sampling for BPM readout
APD	DESY	Dual Channel Signal Stretcher
Fast ADC RTM	SLAC	LLRF ADC Frontend

Available RTMs for SIS8300

SIS8900 Single Ended Input RTM

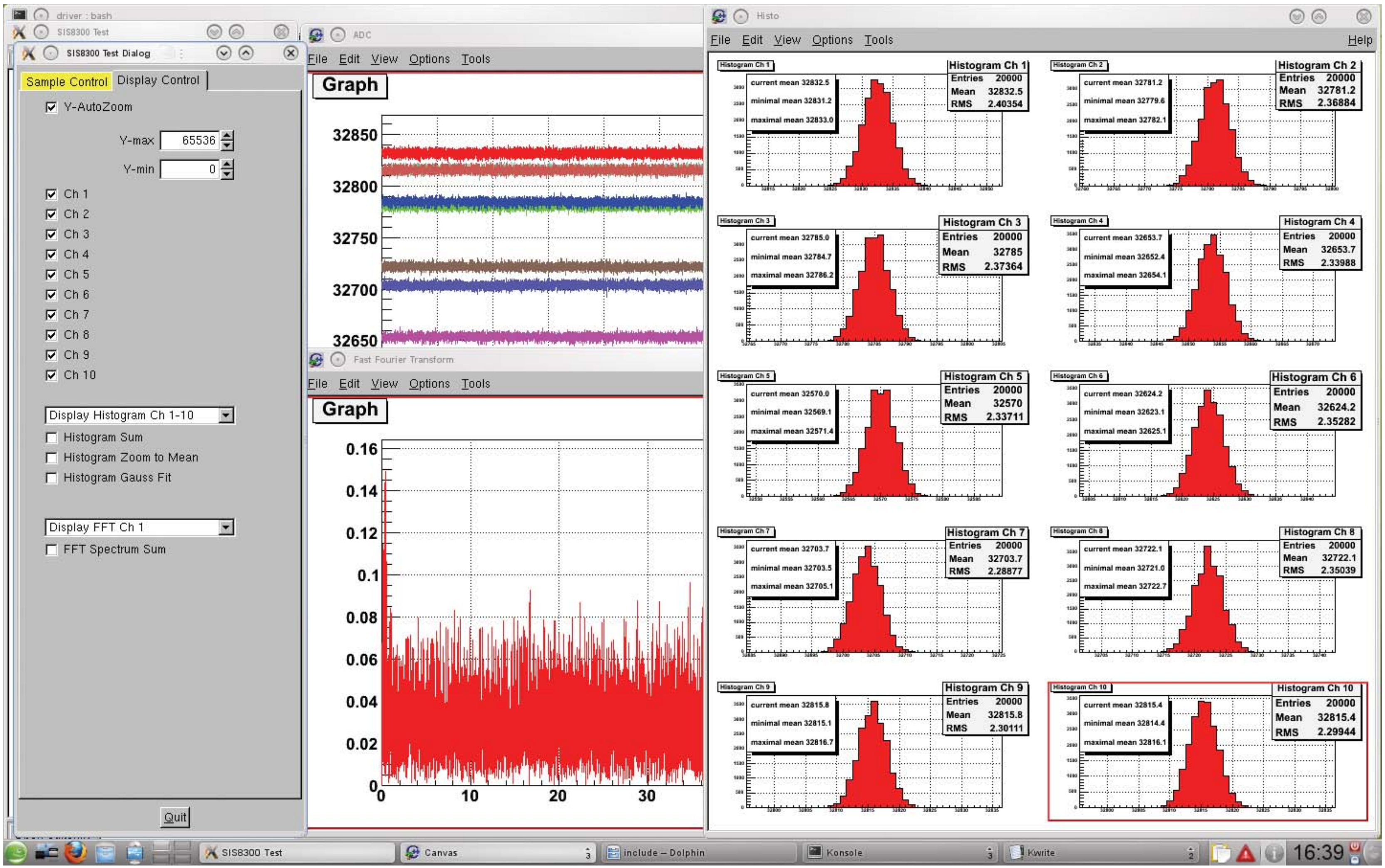
- 10 LEMO 00 connectors (FMB option)
- 50 Ohm input impedance
- -1 V,...,+1 V default input range
- analog signals can be routed to AC and DC input stage
- RJ45 jack for RTM clocks
- RJ45 jack for Digital I/O
- +5V, 250 mA power option for RJ45 jacks
- two metric on board pin headers for 6 LVDS input/output signals each



SIS8900 Application Examples

- SIS8300 Production Tests
- SIS8300/8900 as Standard Single Ended Digitizer
- PTB 10 pm Interferometer Readout (so far SIS3302 VME implementation)
- PTB Delay Line Readout Development (Pulsed Fast Neutron Transmission Spectroscopy)

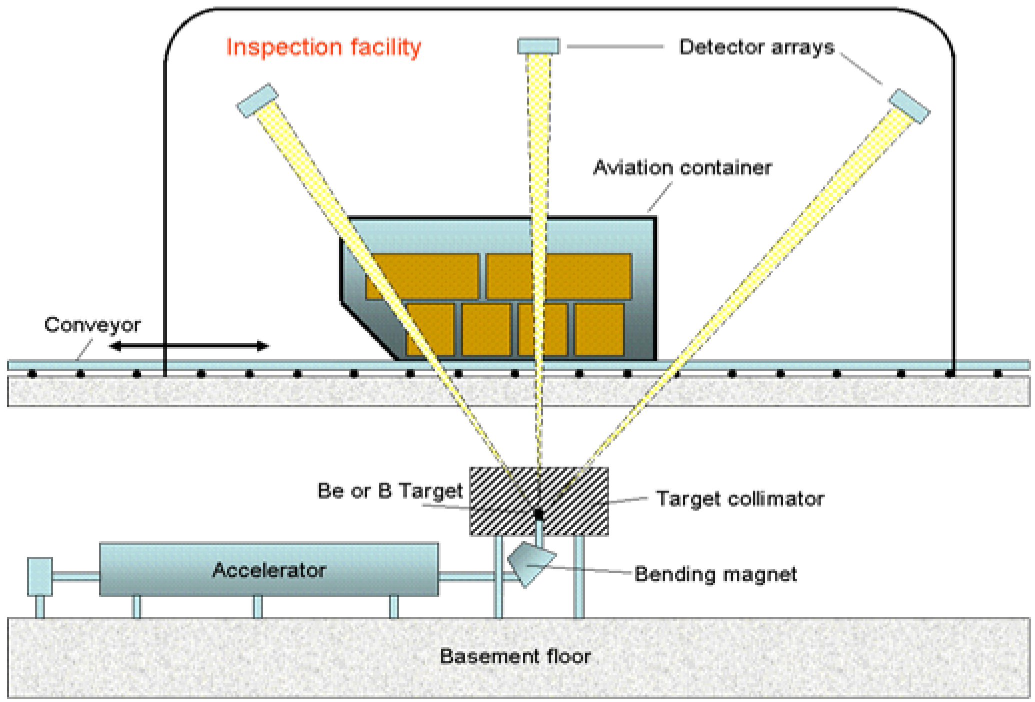
SIS8300/8900 ROOT GUI



Border-crossing security inspection based on Neutron and Gamma Radiography

suitable for inspecting medium-size cargo or passenger vehicles

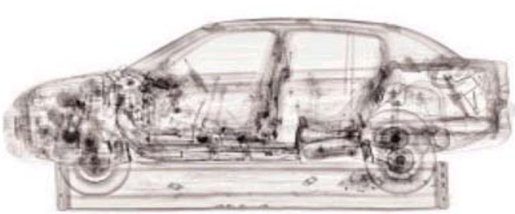
Oversized objects



Schematic view of proposed border-crossing inspection system

Palletized cargo

Air cargo containers

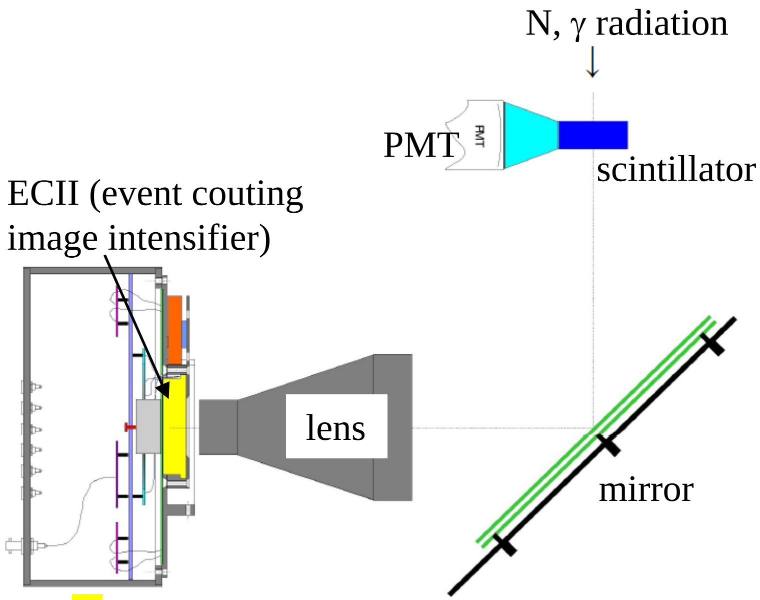


Passenger vehicles

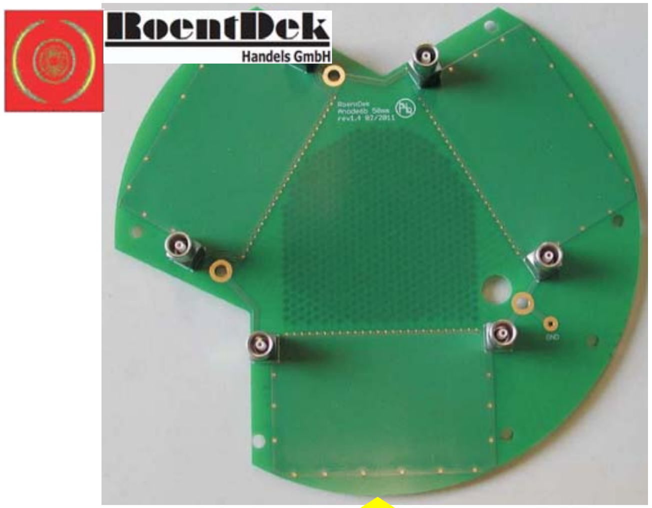
V. Dangendorf

Imaging Detector for PFNTS

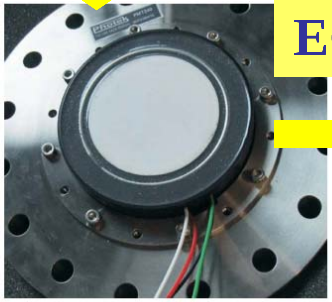
TRECOR: Time-Resolved Event Counting Optical Radiation Detector



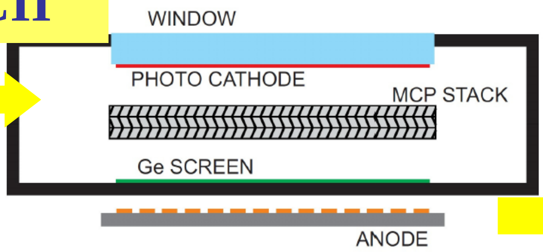
Pickup Electrode and Delayline

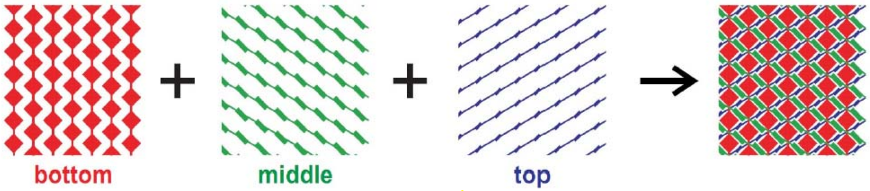


X,Y,Z - 3d pickup electrode



ECII





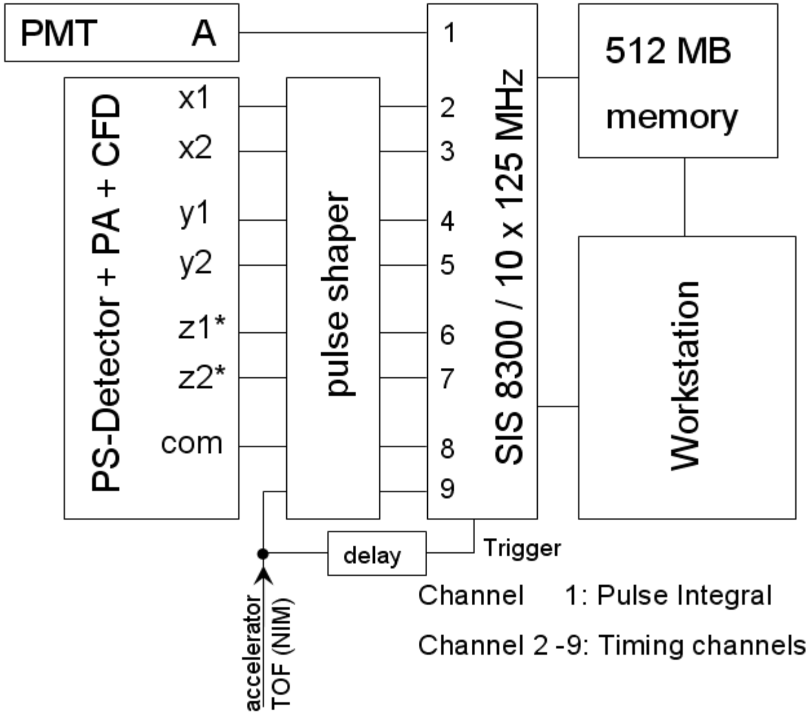
V. Dangendorf

DAQ for TRECOR

- system requires 60 optical readout channels
- each Channel aquires Image (x, y), Time-of-Flight (TOF) and Energy (E_γ) - Parameters
- derived from 8 measured params, mostly time differences < 30 ns
- data rate >2 MHz / optical channel
- online data compression and pre-analysis on DAQ board in scalable system peferably

Concept based on µTCA with SIS8300:

- dT measurement with fine/coarse masurement:
  Fine: amplitude of rising edge
  Coarse: 125 MHz clock of SIS 8300
- Calculation of x(512),y(512),TOF(128), E(16) in FPGA (brackets: parameter resolution in ch)
- Consistency check of parameter set in FPGA
- Histogramming of 4-d Matrix in memory
- Optional transparent mode for Analysis in WS



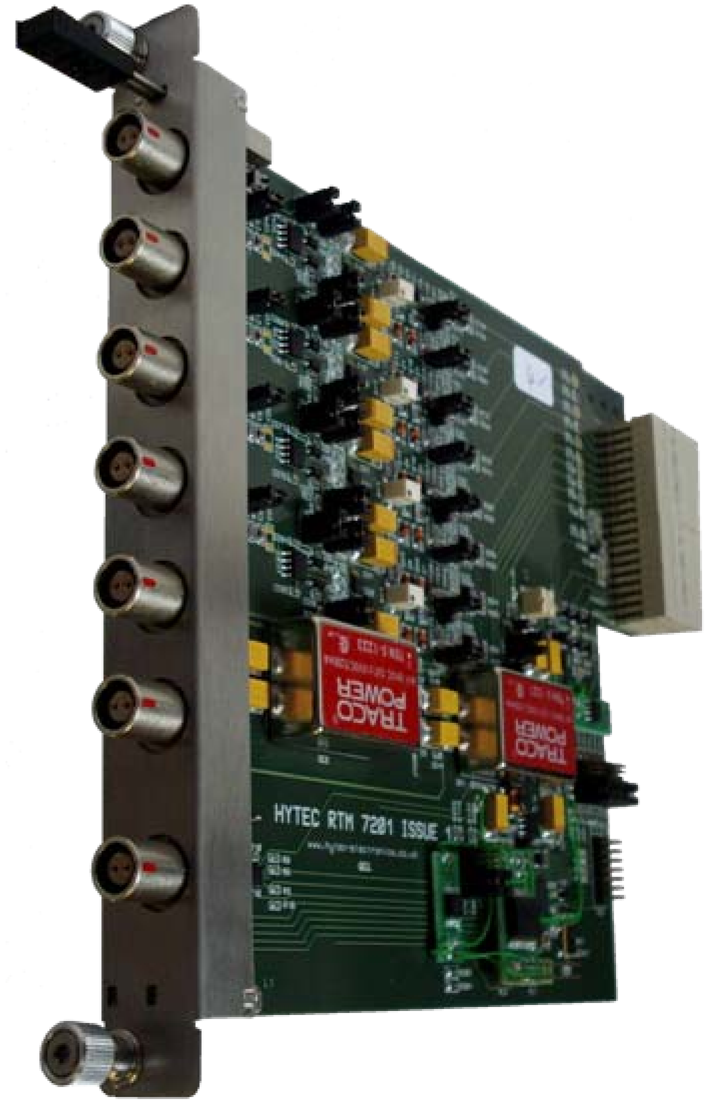
V. Dangendorf

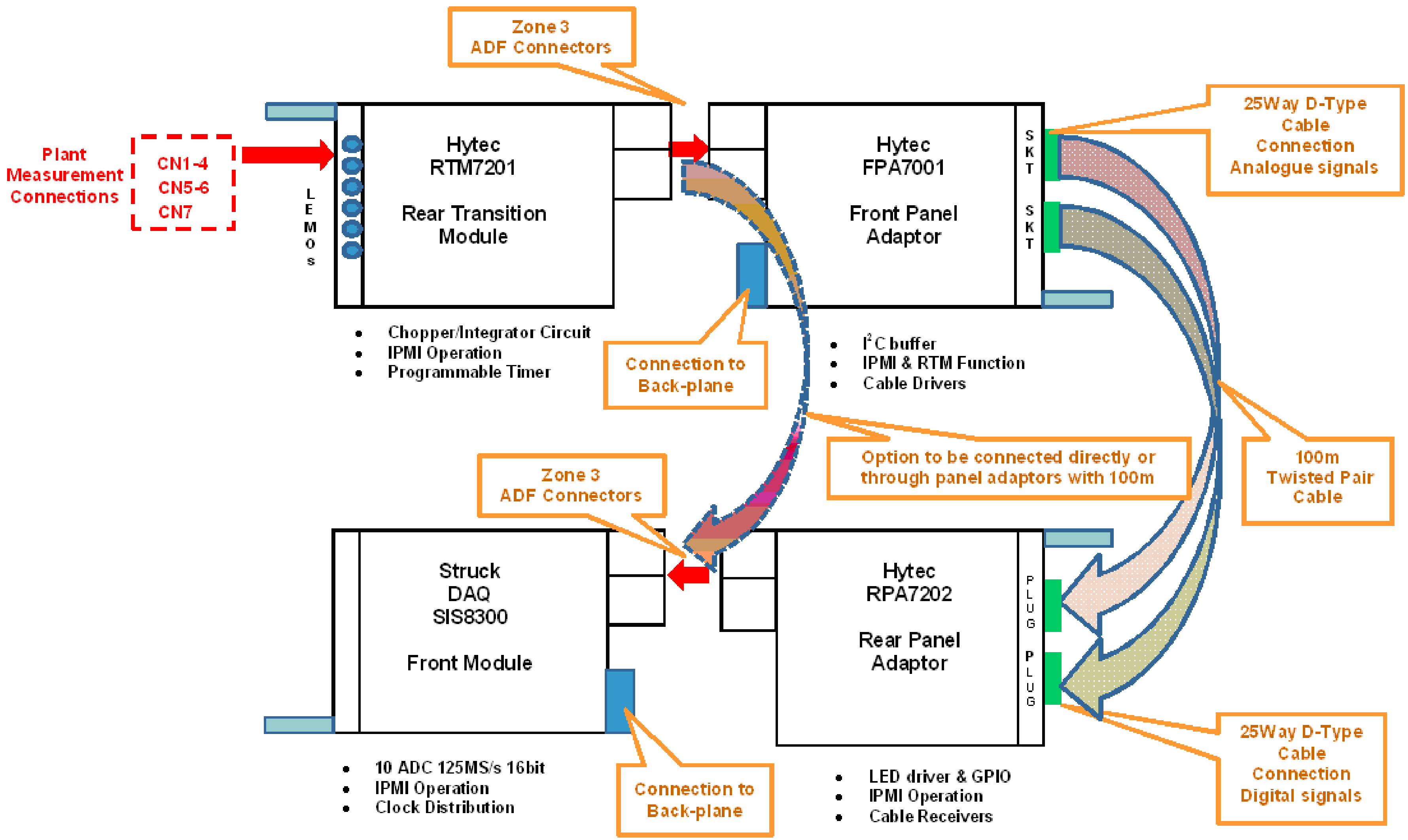
HYTEC RTM7201

ITER magnetic sensor readout
4-channel signal modulator

Harsh/Noisy environment →
Signal conditioning RTM

with driver/receiver AMC/RTM
(direct SIS8300 connection option)

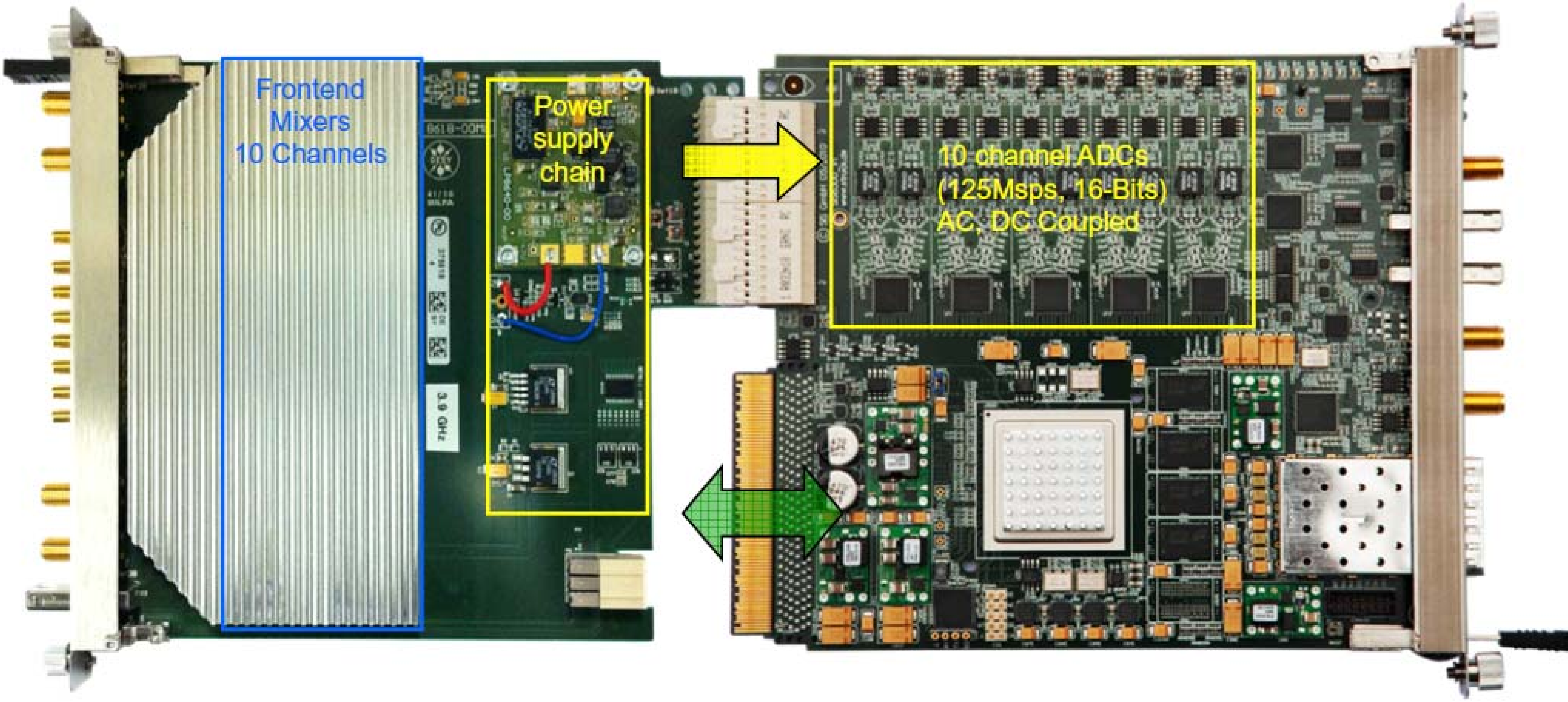




Block Diagram of the Complete System

DWC8300/SIS8300

- 10-channel Down-Converter
- Digitizer, Partial Vector Sum



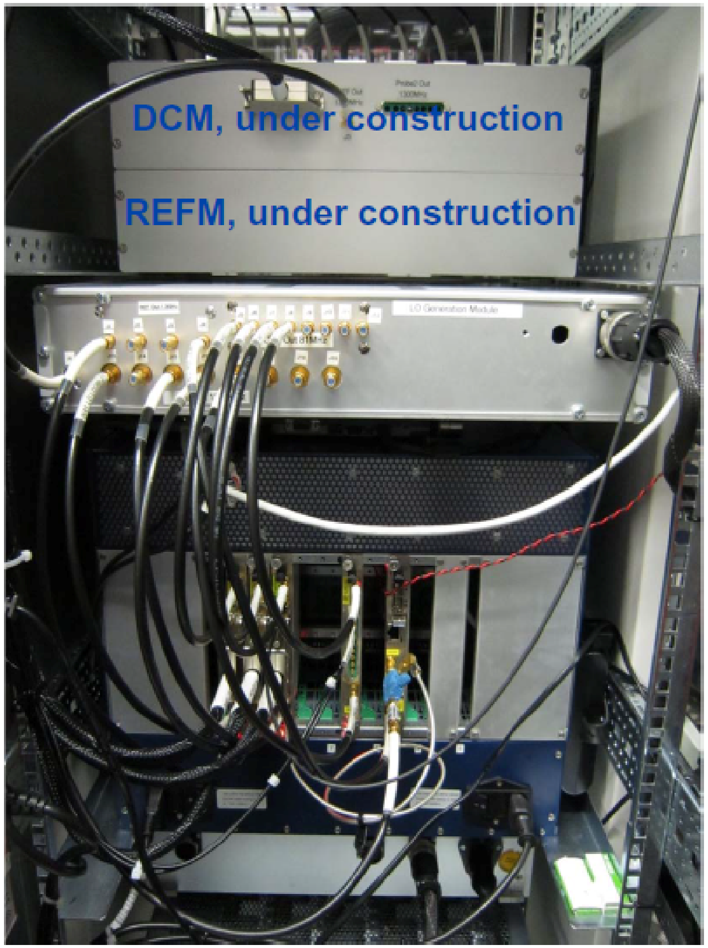
- 10 channel field detection
  (1.3GHz, 3.0GHz, 3.9GHz)

- 10 channel ADCs (125Msps, 16-Bits)
- FPGA partial cavity vector sum
- Low latency links via uTCA-backplane

Flash Injector Rack Installation

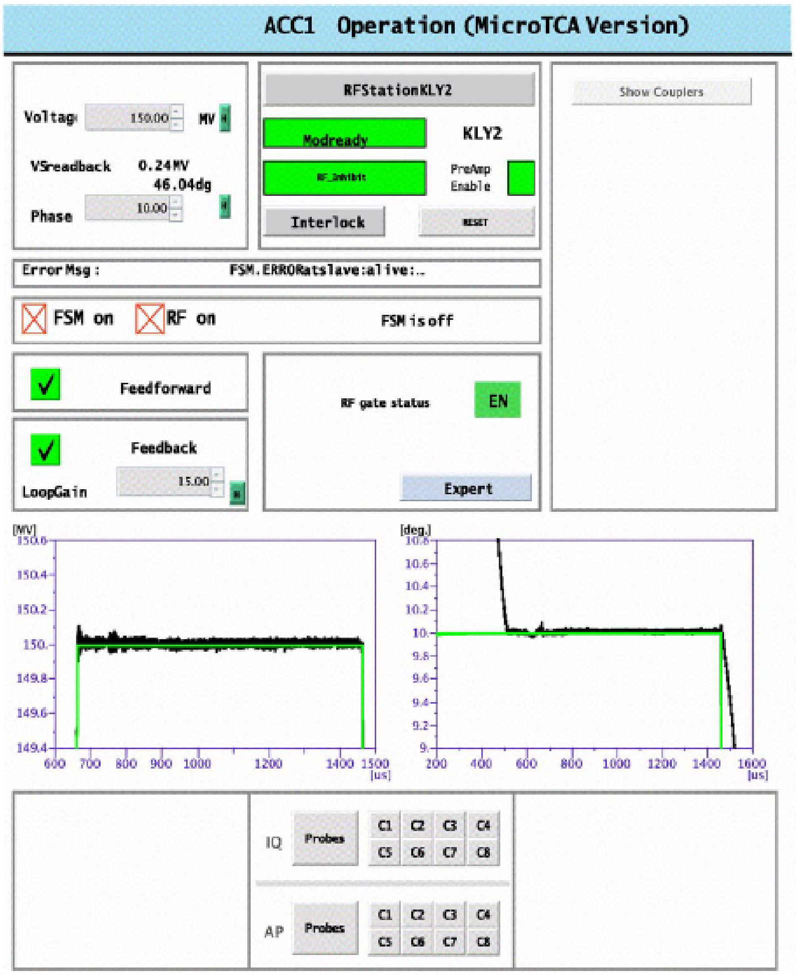
- uTCA Prototype Front view

- uTCA Prototype Rear view

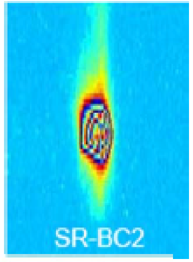


FLASH Operation

FLASH operation :

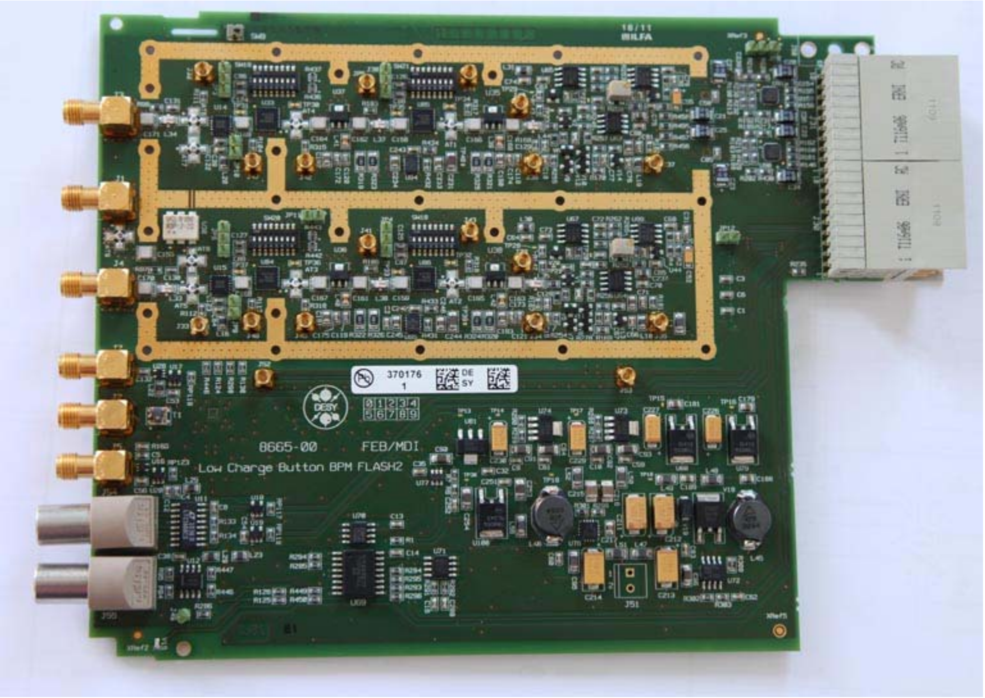


On-crest energy stability :



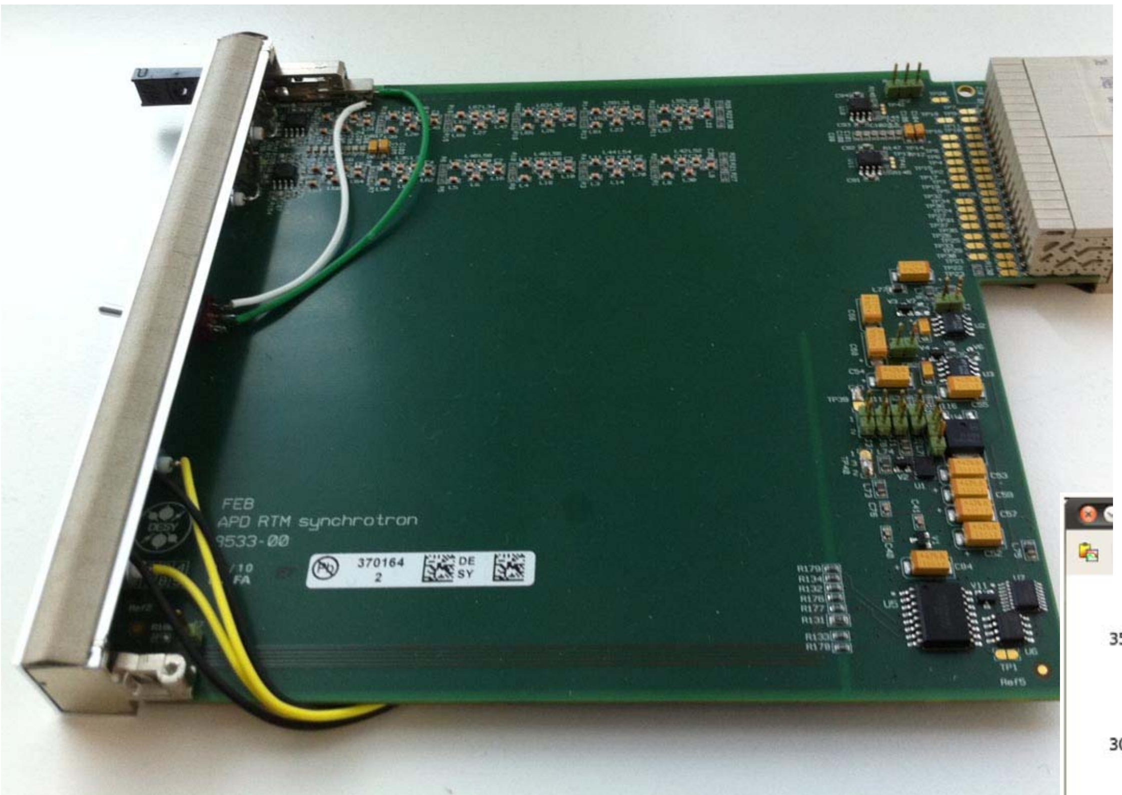
→ Energy stability dE/E=0.5E-4.

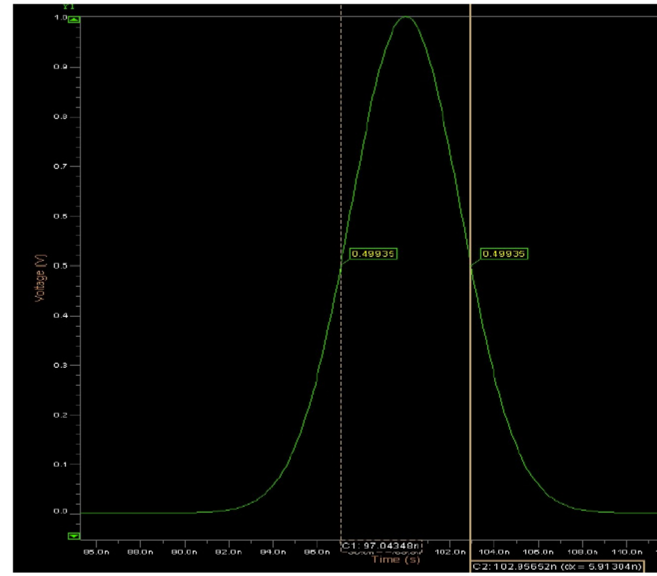
DESY BPM RTM



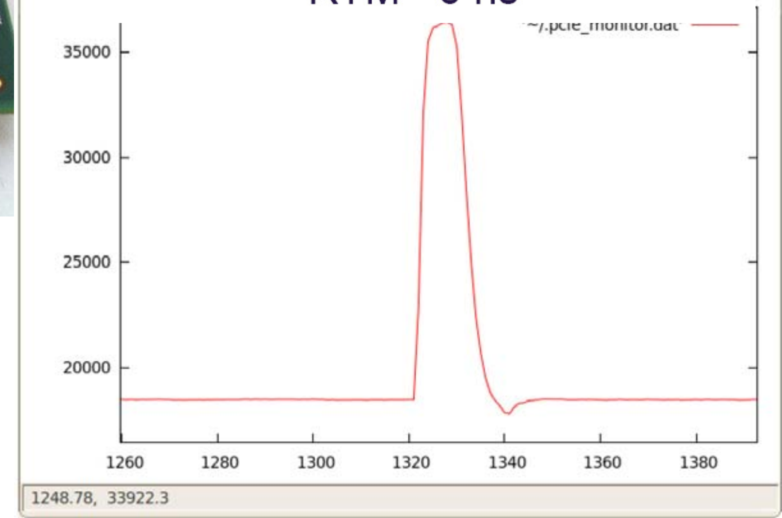
Interleaved Sampling
50 pC resolution target
Frank Schmidt-Föhre, Bastian Lorbeer

DESY APD Stretcher RTM





APD Pulse before RTM ~6 ns



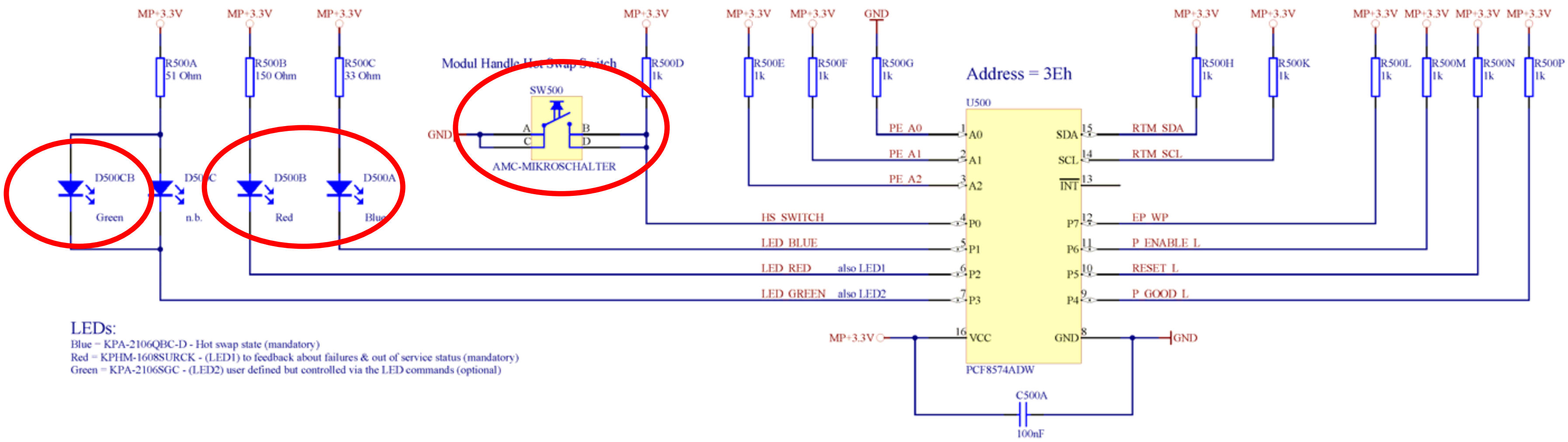
Dual channel signal stretcher

Petter Göttlicher, Chris Youngman

Build your own RTM? Partial Requirements

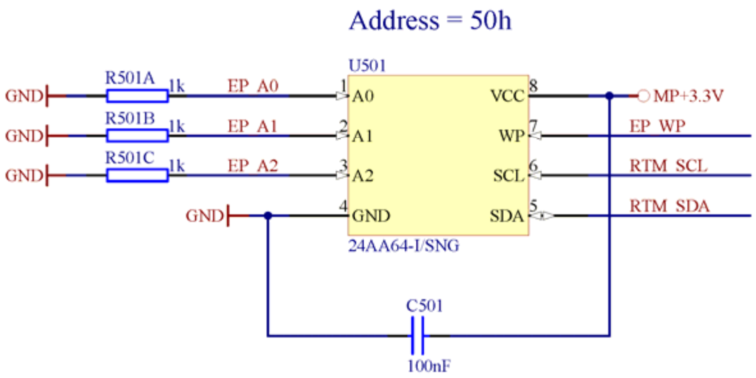
- I^2C Bus
- AT24C32A compatible serial EEPROM (connected to the fron AMC I^2C port and at address 0x50)
- Blue hot swap LED, LED1, optional LED2
- Hot swap ejector handle (AMC MMC readable)
- The µRTM shall provide at least one temperature sensor (AMC MMC readable)

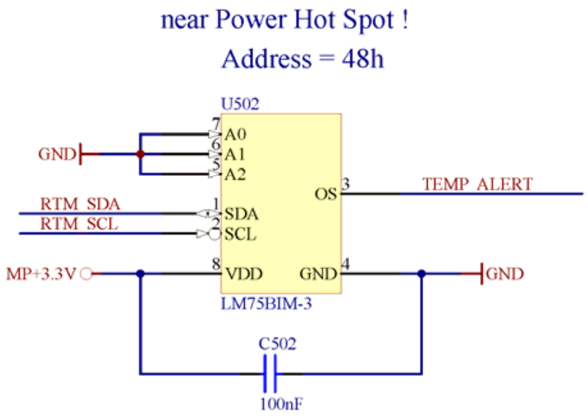
SIS8300 Compatible RTM Management - I2C Port Repeater



Note: Later drafts and final spec.:
µRTMs that control the LEDs via I2C should use LED drivers with programmable blink rate and duty cycle
→ can be accomodated with change in SIS8300 management code as needed

SIS8900 RTM Management EEPROM and Temp Sensor





SIS8300 Compatible RTM Management – Identifier Record

The EEprom shall contain any relevant device information (FRU records) about the RTM (refer to PICMG AMC.0). Additionally the EEprom shall contain the new record types defined in PICMG MTCA.4.

In order to be able to decide whether a connected RTM is compatible to the SIS8300 the RTM record shall contain one of the Zone 3 Identifier records listed in the table below.

Supported Zone 3 Identifier Records (Interface Identifier OEM):

IANA PEN (Private enterprise number)	Zone 3 OEM record	Descripton
0x0092BD (37565)	0x83000001	SIS8300 Zone3 - v1 compatibility
0x00053F (1343)	0x08020000	DESY DWC Zone3 compatibility

http://www.iana.org/assignments/enterprise-numbers
0x0092BD (37565)
Struck Innovative Systeme GmbH
Thorsten Fritzke thorsten.fritzke&struck.de

IANA: Internet Assigned Numbers Authority

Outlook

- SIS8300-L Digitizer development under way, Virtex 6 (XC6VLX130T-2FFG1156C) instead of Virtex 5 (MGT link speed), DDR3, DAC to Z3,…
- Multi GSPS 12-bit MTCA.4 Digitizer in 2013
- Differential input RTM development upon request

Summary

- SIS8300/DWC8300 MTCA.4 Digitizer-Downconverter combination meets XFEL LLRF specification
- SLAC LLRF ADC Frontend (talk by Zheqiao Geng, SLAC)
- BPM and APD stretcher RTMs
- ITER RTM Development (HYTEC)
- Single ended SIS8900 RTM
- Substantial progress since Valencia NSS xTCA Workshop

µTCA/MTCA.4 Ecosystem

- good feedback during IPAC12
- user base increasing (recent ESS PO)
- some 50 SIS8300 and 10 SIS8900 in field
- availability of standard hardware increasing

You will want to keep in mind that a learning and introduction curve was present in other standards -like VME- as well

Acknowledgements

The SIS8300 was developed in co-operation with DESY under ZIM Förderkennzeichen 2460101MS9

We‘d like to extend our special thanks to Kay Rehlich from DESY for the good atmosphere and the assistance throughout the development and Frank Ludwig from DESY for his input and continued support for improvements on the analog side in the V1 to V2 revision transition and beyond

→ SIS8300-L

Vendor Exhibits

- ELMA 6 slot MTCA.4 crate
- NAT MCH
- Kontron AMC5020 CPU
- SIS8300 Digitizer
- SIS8900 RTM

CERN ROOT SIS8300 demo application
under LINUX
(and Rigol signal generator)

Questions/Discussion

GL ISO 9001

GL Systems Certification