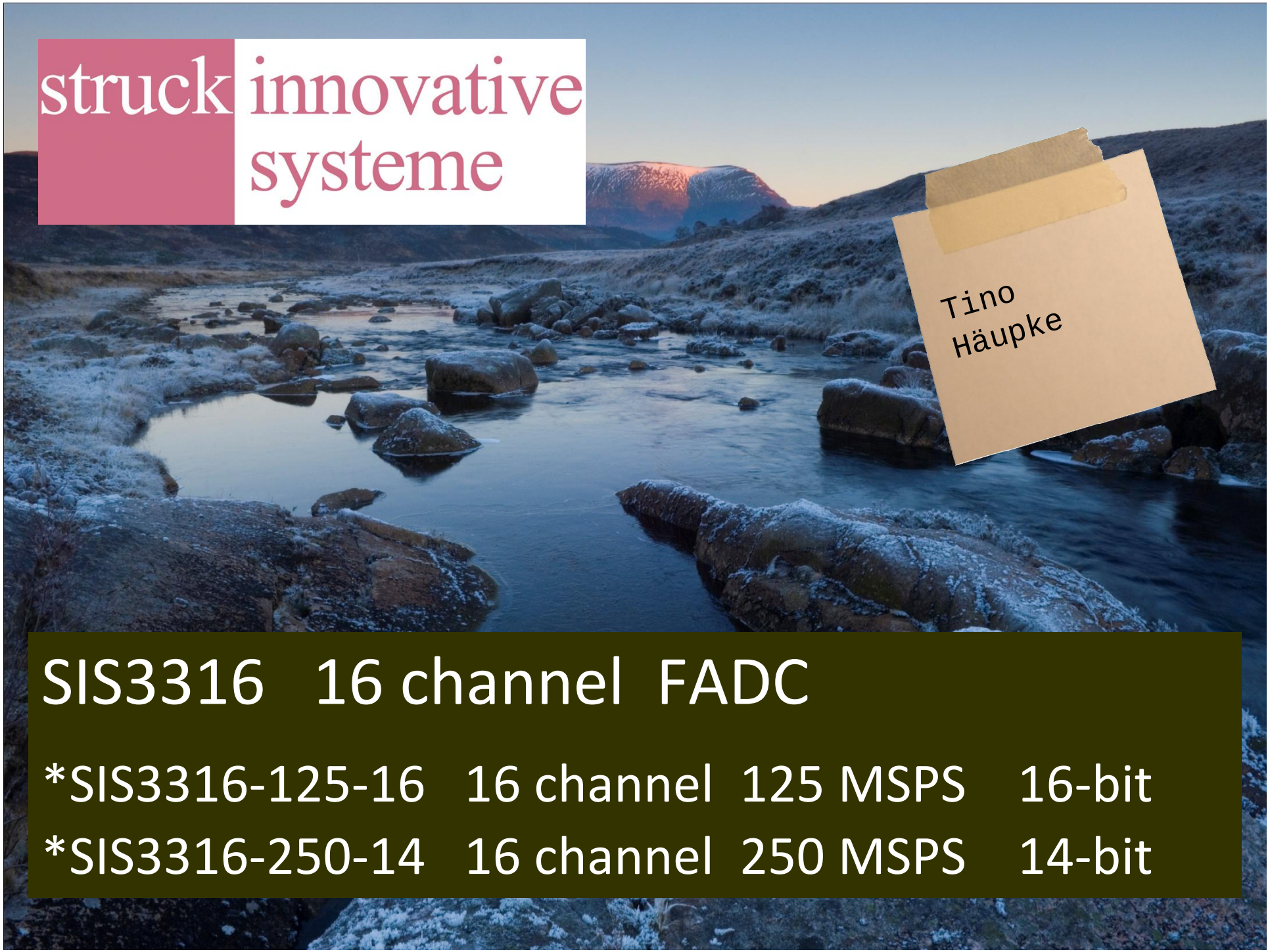
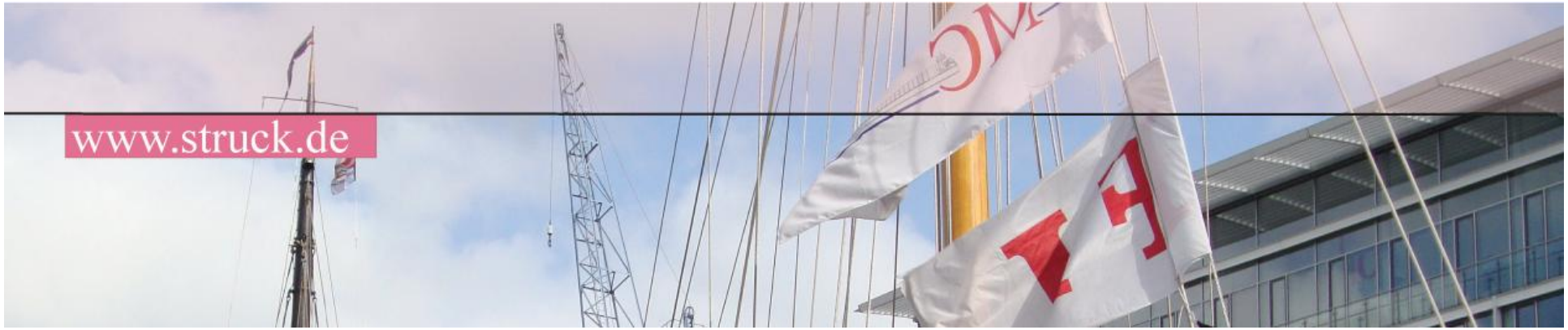


SIS3316 16 channel FADC

*SIS3316-125-16 16 channel 125 MSPS 16-bit

*SIS3316-250-14 16 channel 250 MSPS 14-bit



based in Hamburg Germany

in operation since 1998

9 employees

customer base

~ 230 worldwide

GL ISO 9001

GL Systems Certification

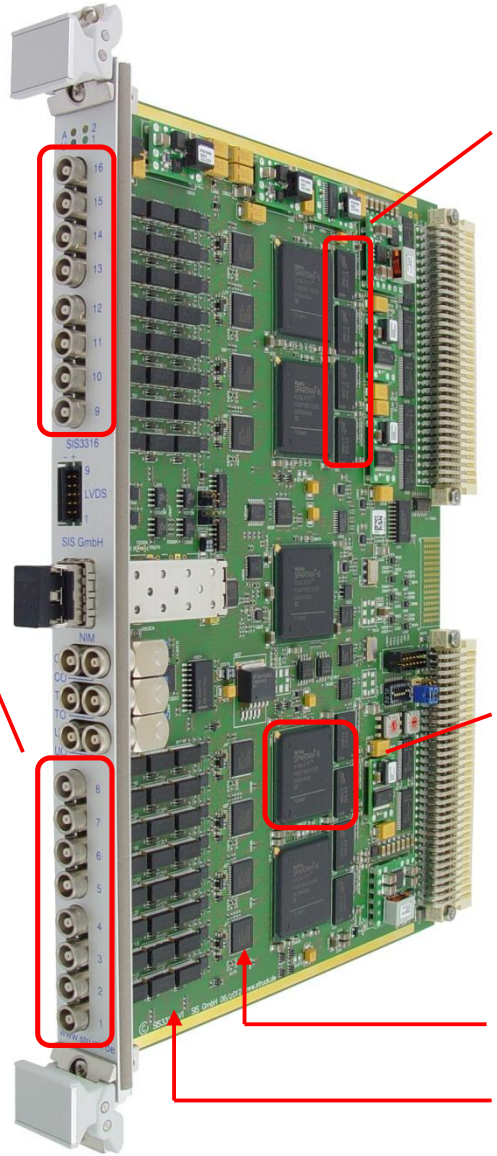
SIS3316 16 channel FADC

16 Analog Input Connectors

- Programmable Input Termination
• 50 Ohm
• High Impedance

- Programmable Input Range
• 5V
• 2V

- Programmable Analog Offset (DAC)
-> variable Input Range from +5V/0V to 0V/-5V
-> variable Input Range from +2V/0V to 0V/-2V



DDR3 Memory

4 x 2 x 256 MByte = 2GByte

• 512 MByte / 4-channel group
• 128 MByte / channel

• 64 MSample / channel

ADC FPGA: Xilinx Spartan 6
XC6SLX75T-3
-compatible options:
* XC6SLX100T
* XC6SLX150T

Application Firmware

250 MSPS 14-bit ADC or
125 MSPS 16-bit ADC

Impedance/Range Relays
and Offsets (DACs)

SIS3316 16 channel FADC

Frontpanel BLVDS Bus

- Clock distribution
- Sample control
- Trigger
- Timestamp clear
- …….

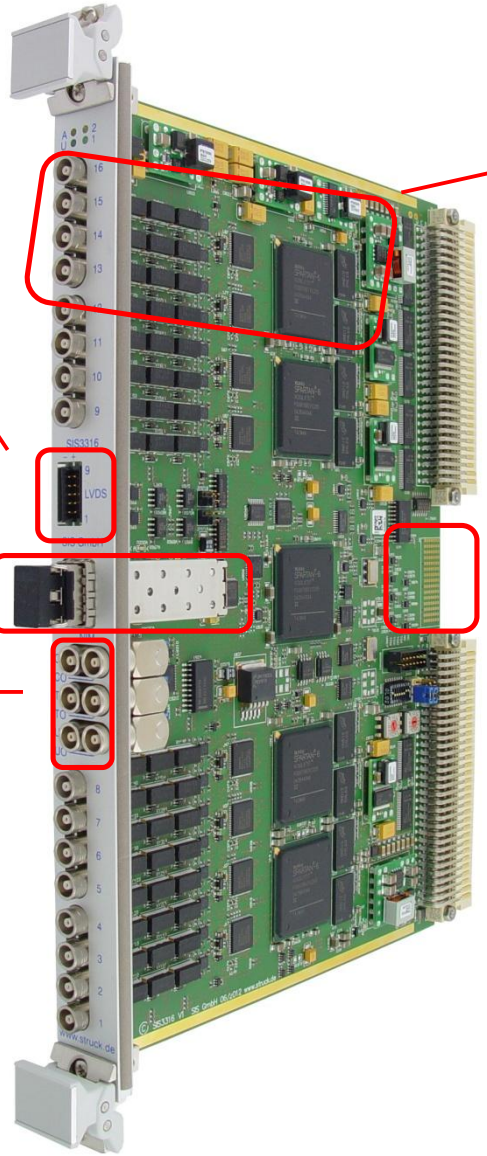
SFP Cage

- Gigabit Ethernet
- Multi-Gigabit optical link connection

NIM Control In/Output

- 3 Inputs
- Input 1:
  Sample Clock or function depends on Firmware
- Inputs 2/3:
  functions depend on Firmware

- 3 Outputs
- Output 1/2/3:
  functions depend on Firmware

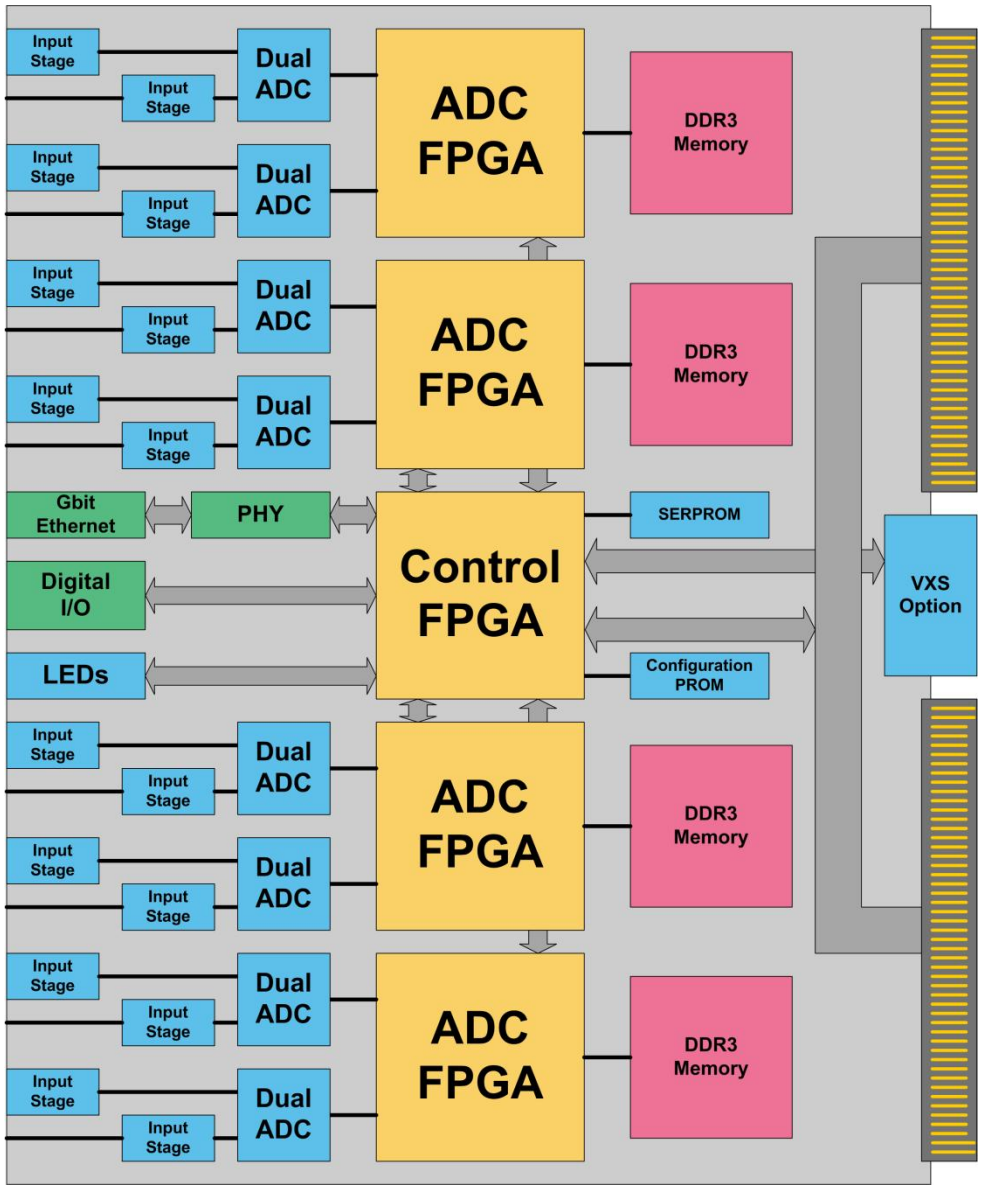


4 channel ADC group

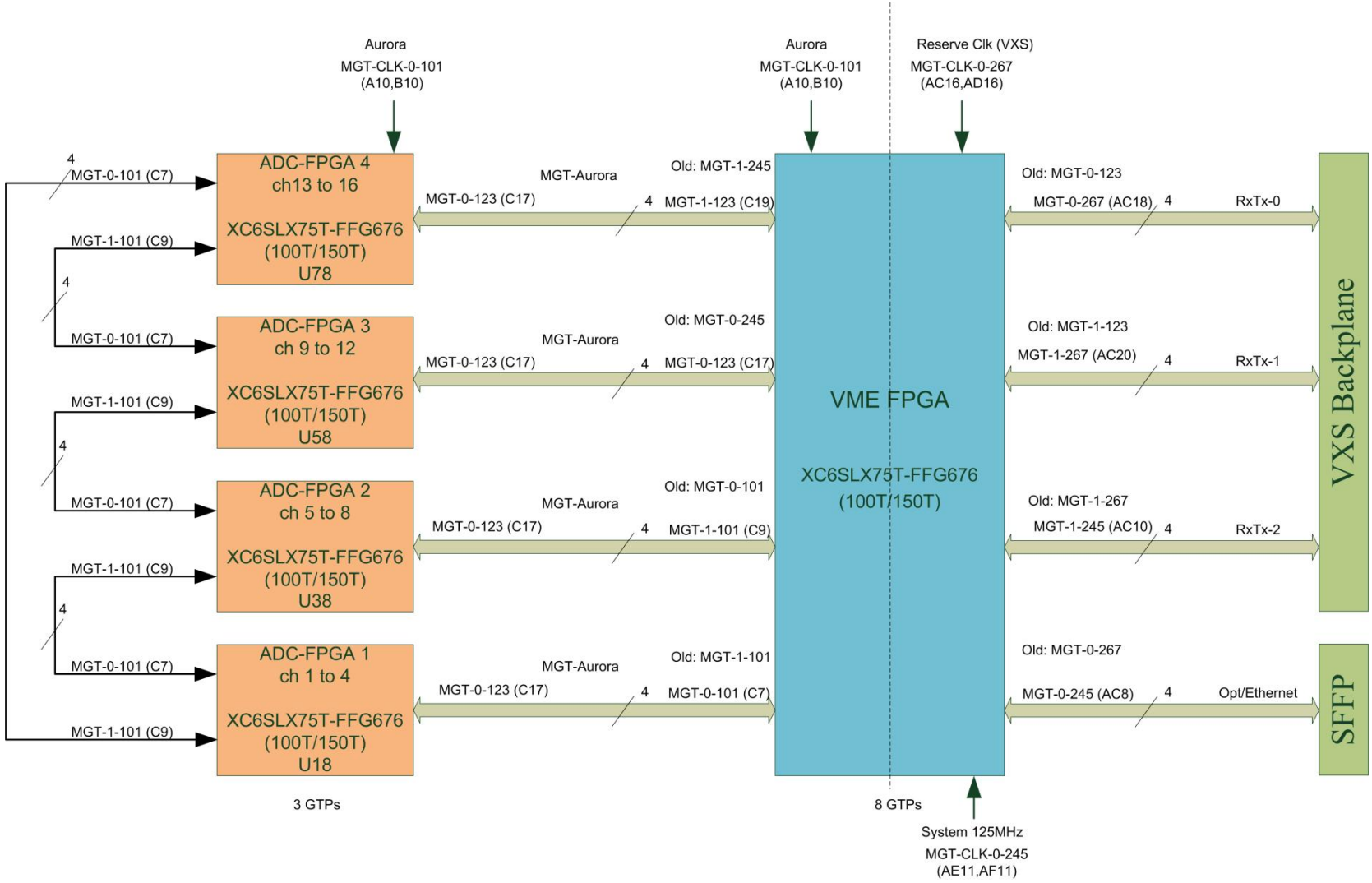
- 4 channel inputs
- 1 FPGA Spartan 6
- 512 MByte DDR3 Memory

VXS Connector space

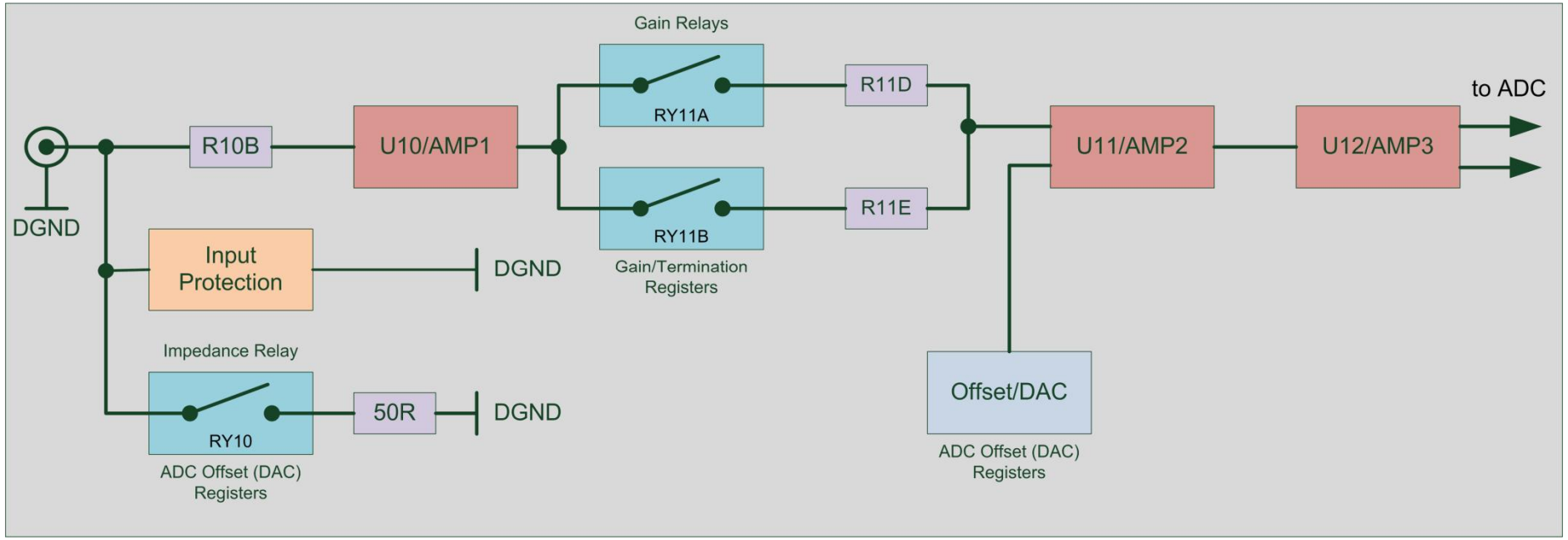
SIS3316 Block Diagram



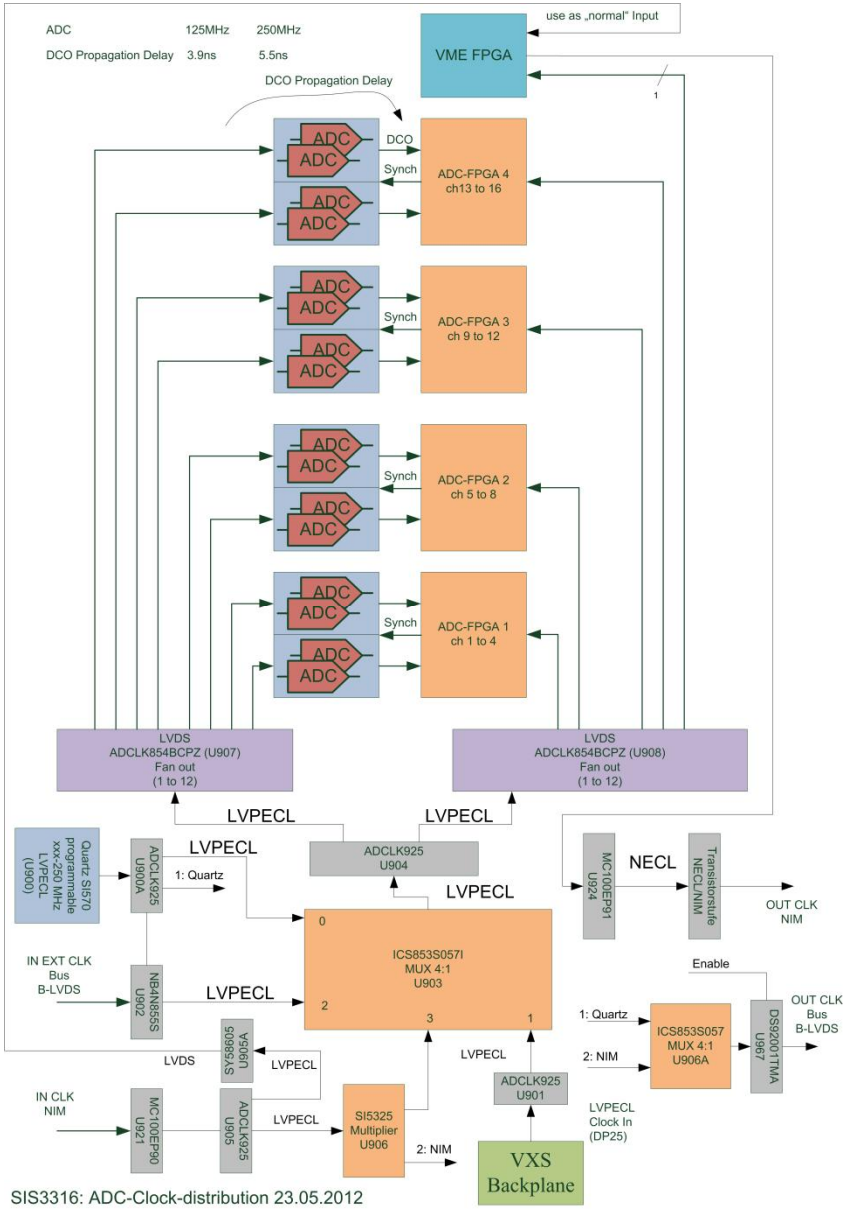
SIS3316 MGT-Links connections



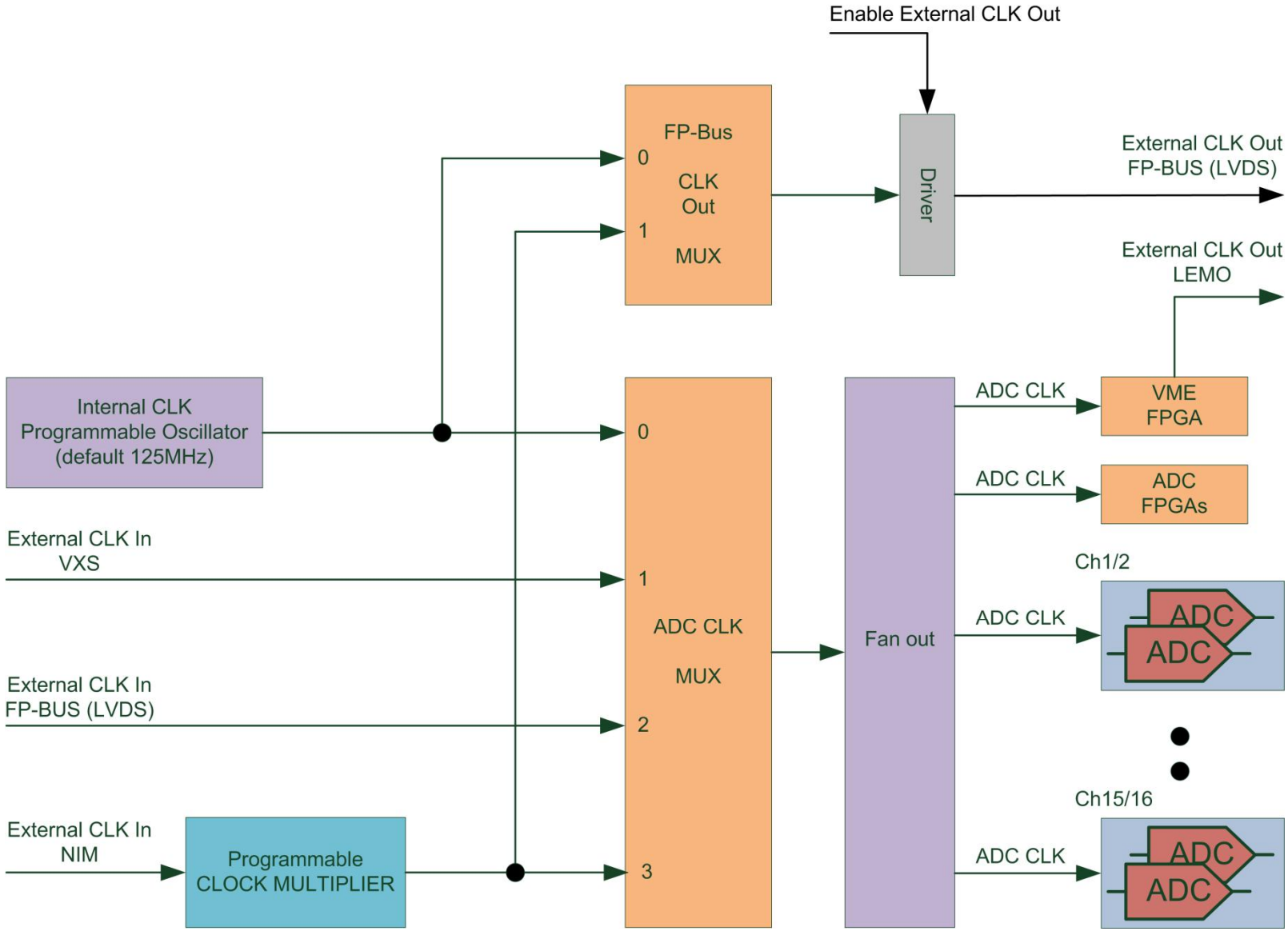
SIS3316 Analog Input Stage



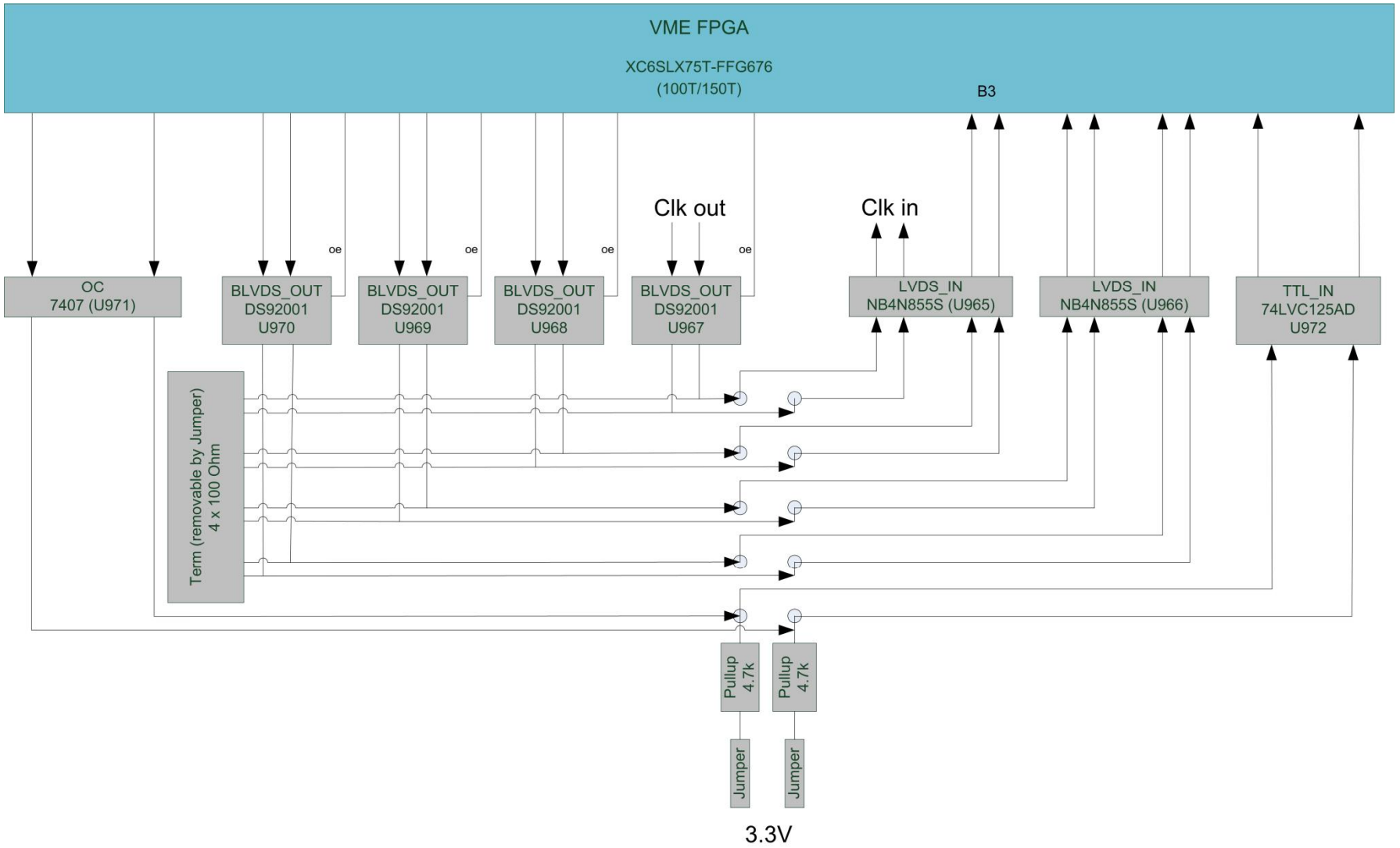
SIS3316 Sample Clock distribution



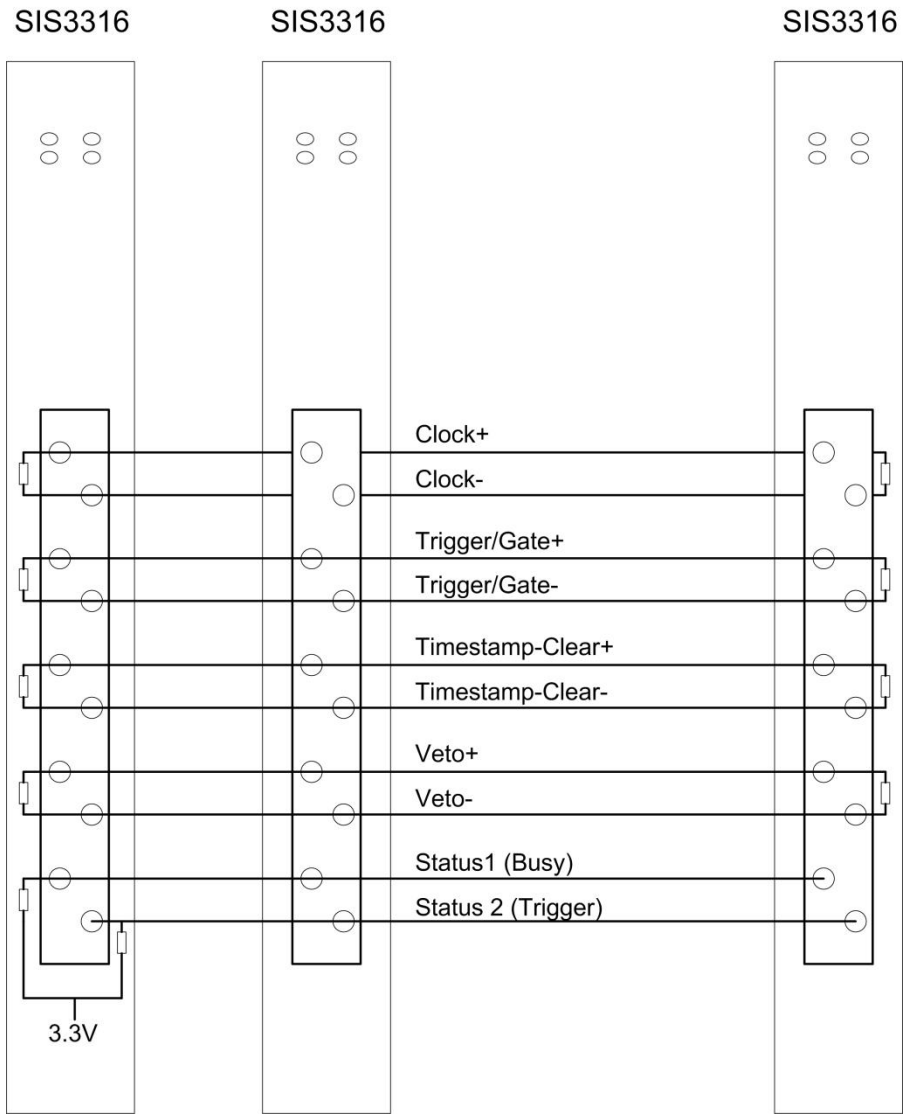
SIS3316 Sample Clock programming



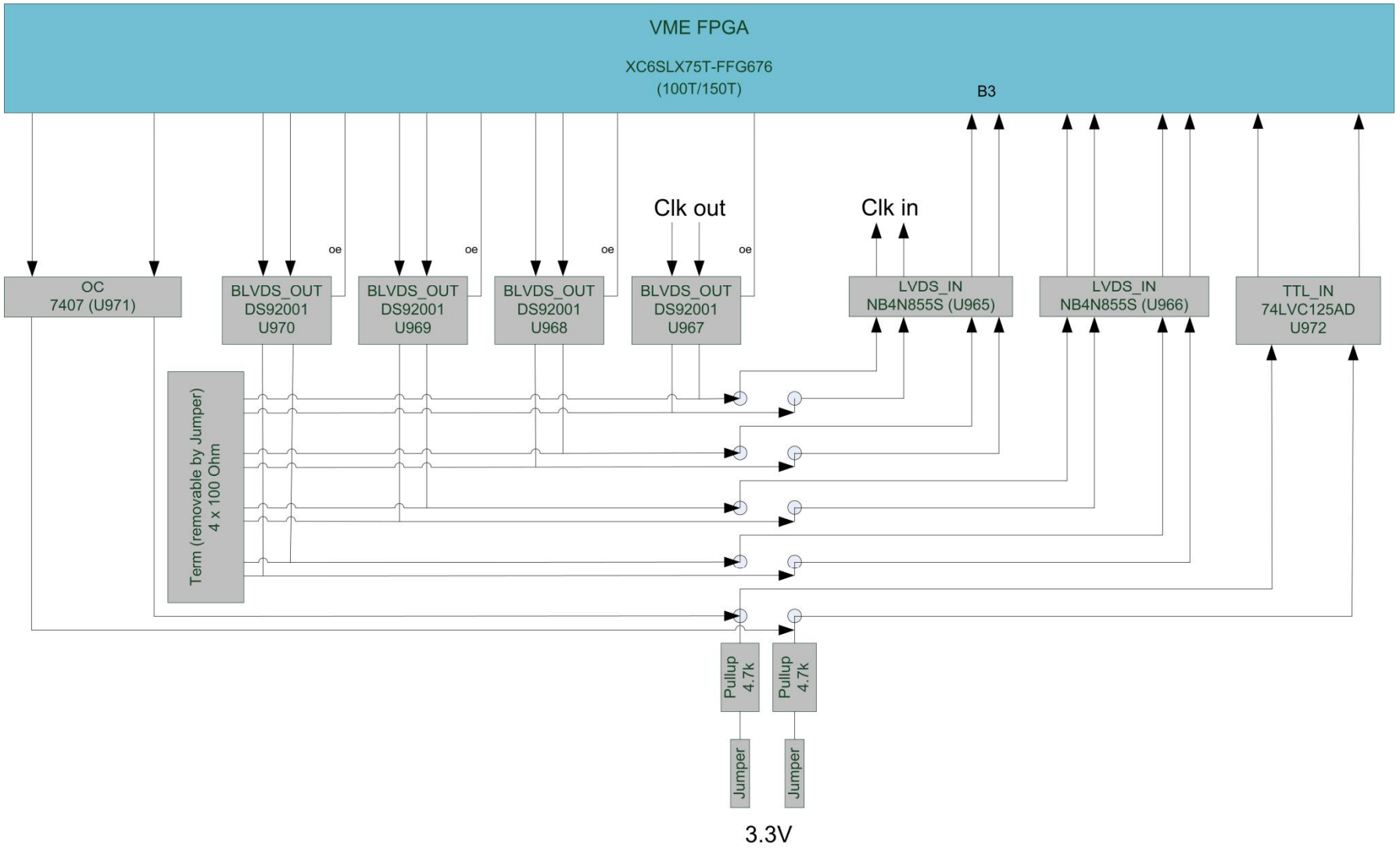
SIS3316 Frontpanel BLVDS-Bus



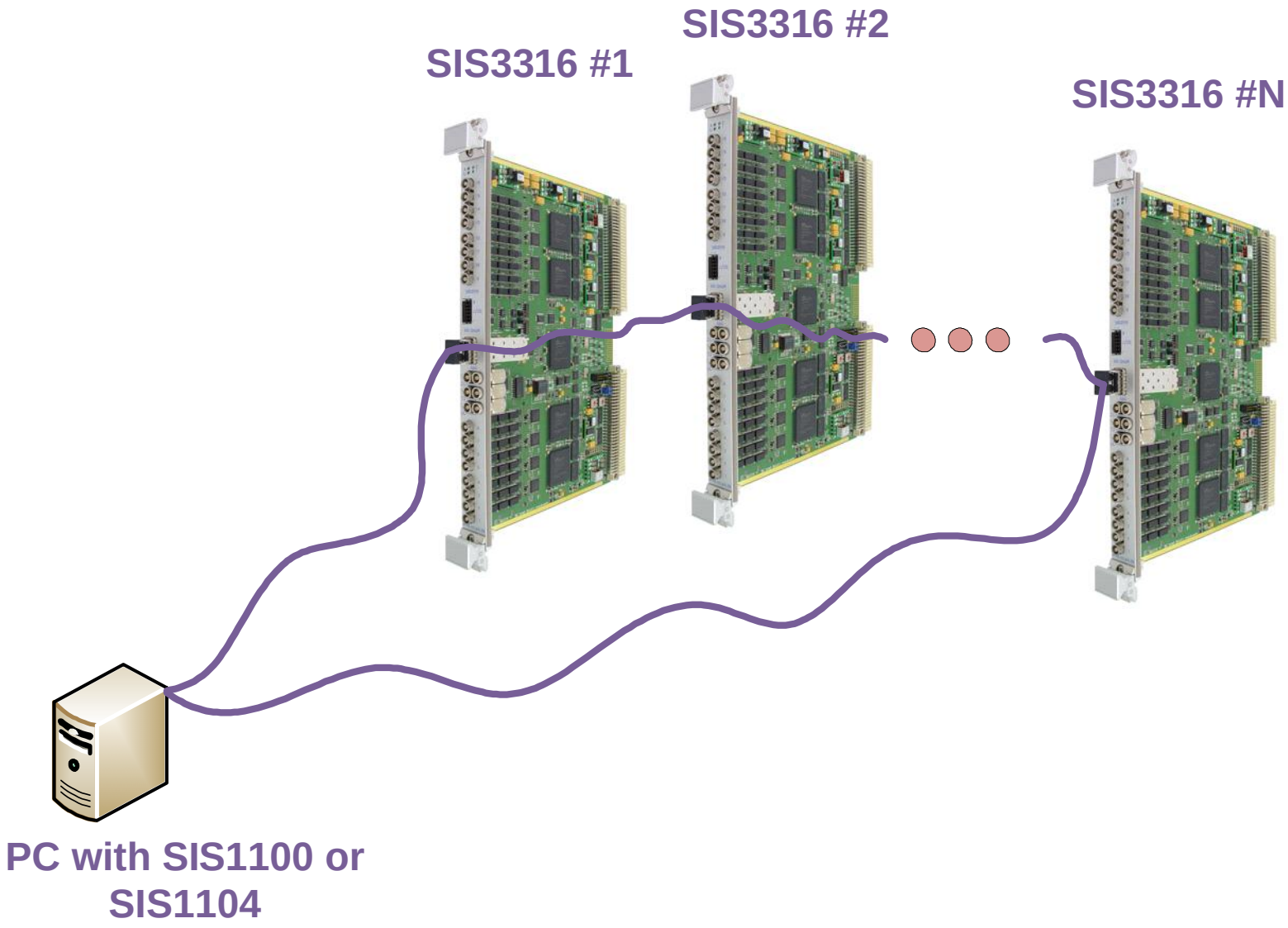
Frontpanel BLVDS-Bus application example



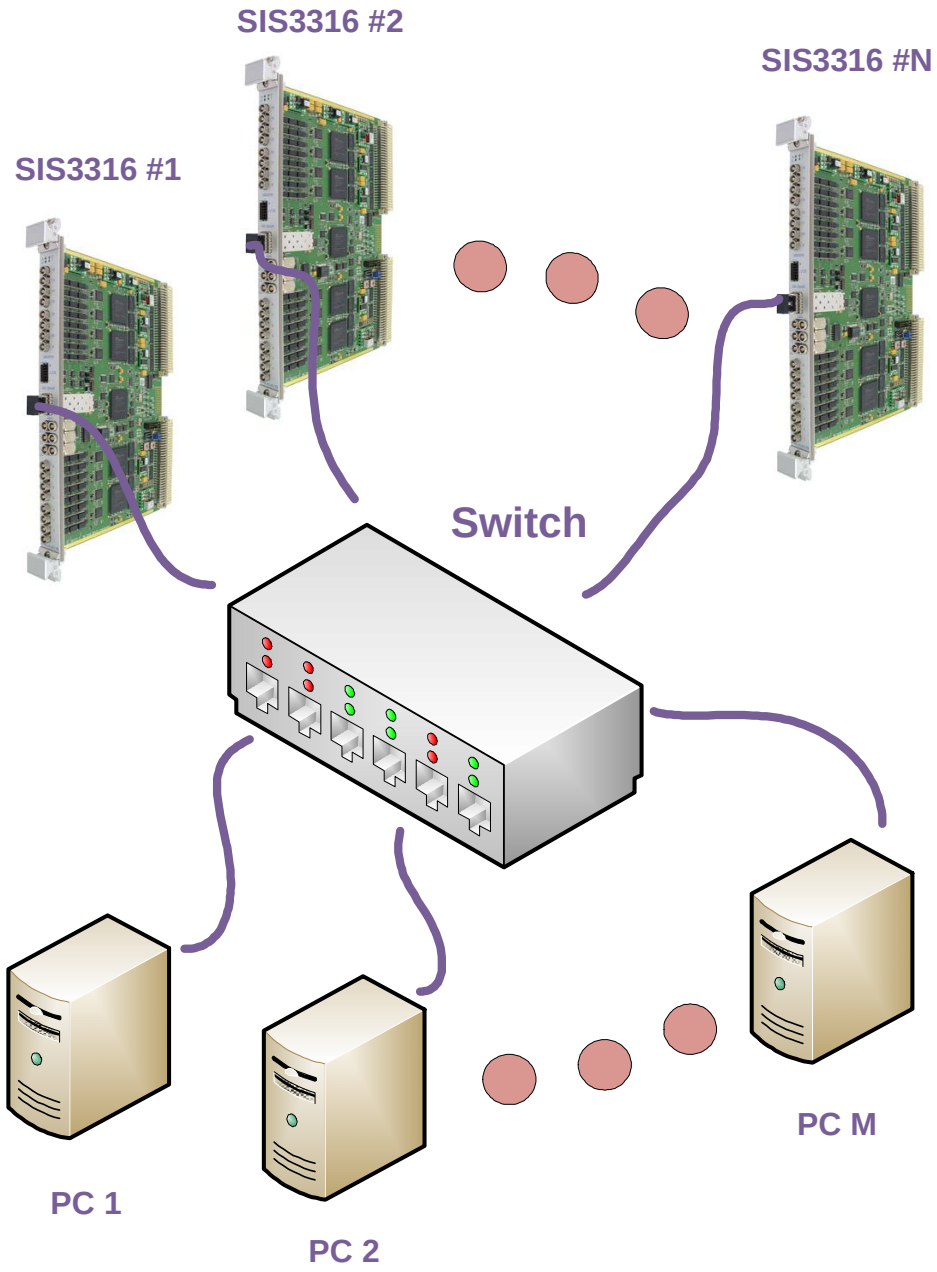
SIS3316 Frontpanel BLVDS-Bus



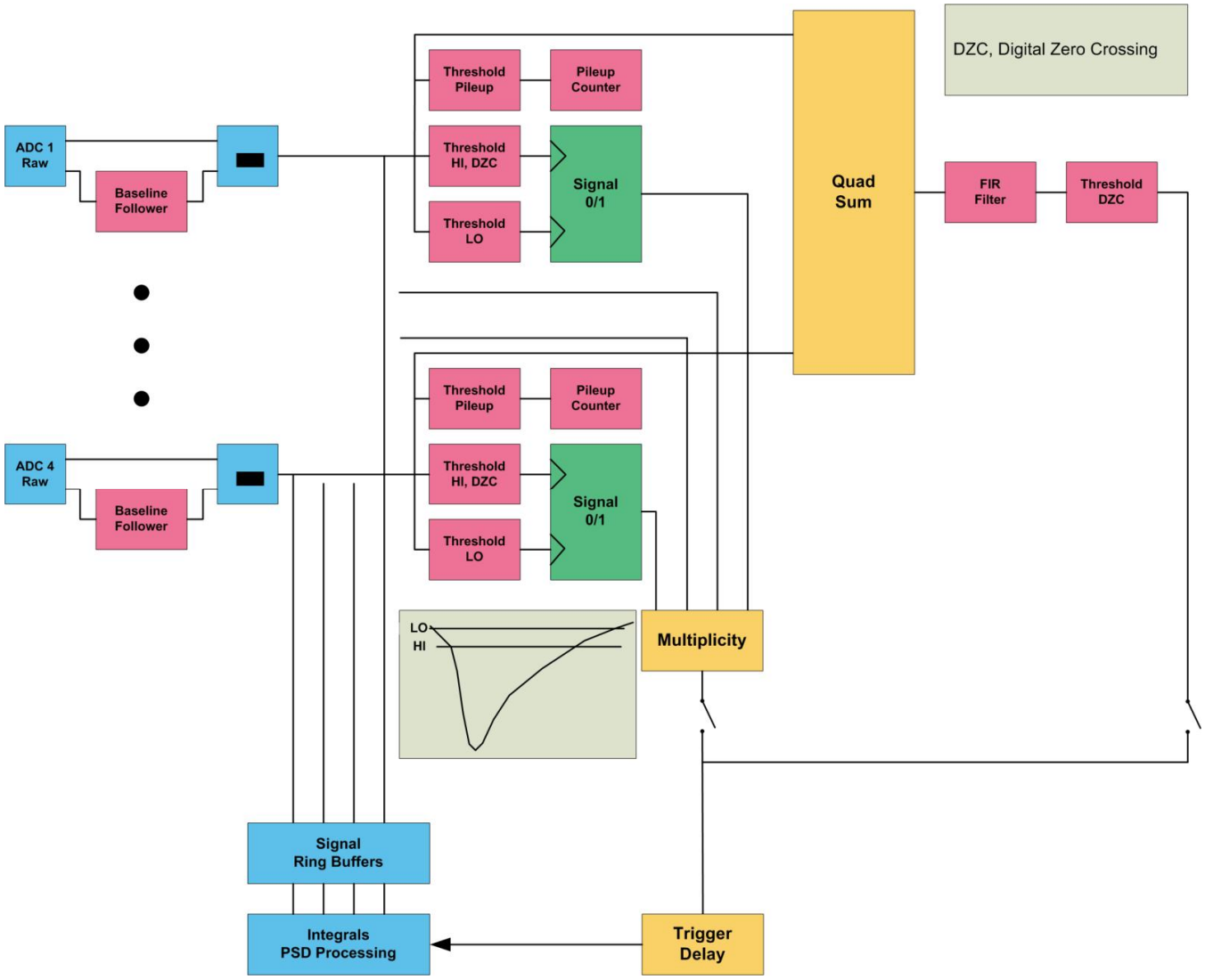
SIS3316 readout with optical fiber ring
#03145 FTLF8524P2BNV



SIS3316 readout with Ethernet
#04333 FCLF-8520-3

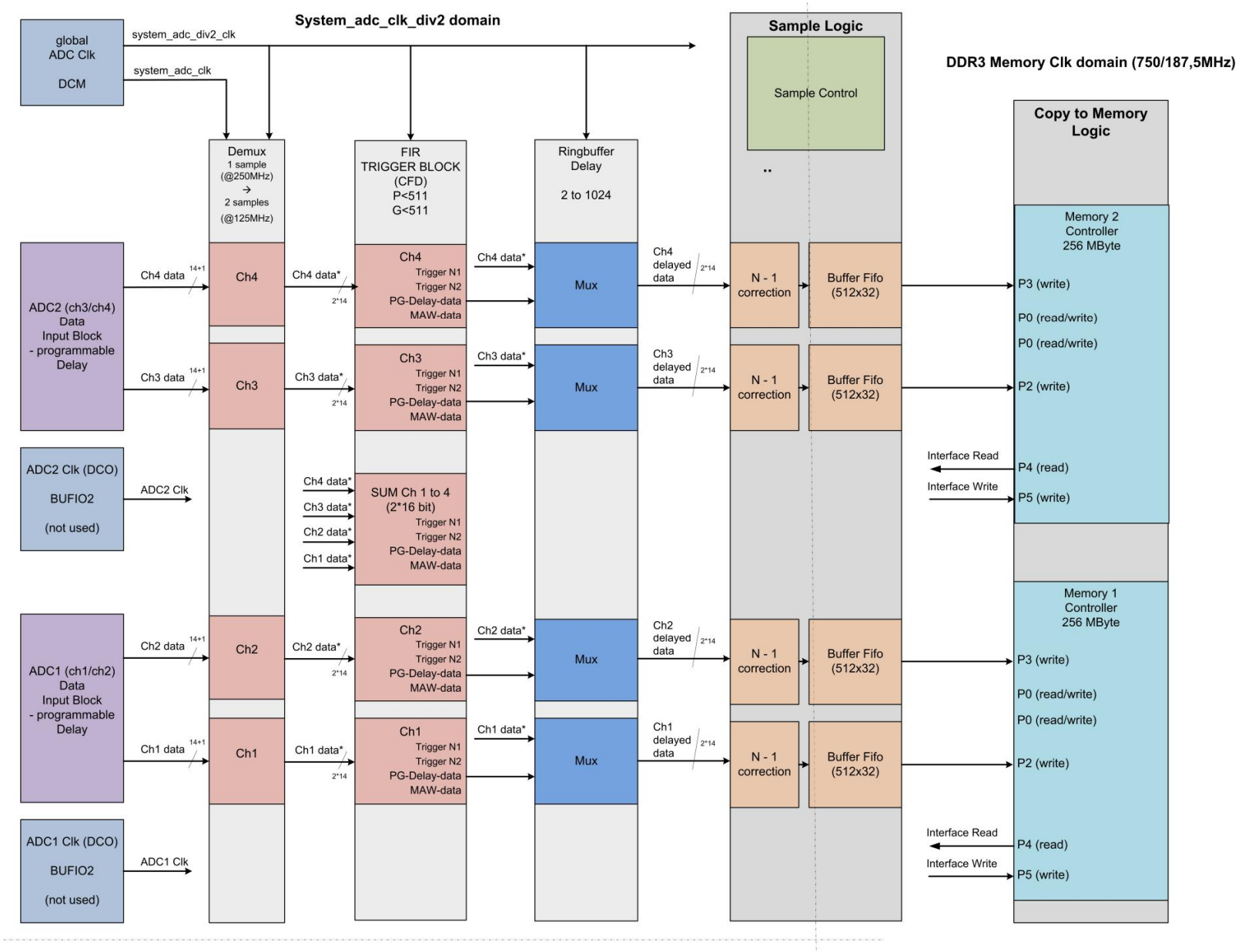


ADC FPGA Firmware Project Definition



Status of ADC FPGA Firmware Implementation

19-08-2012



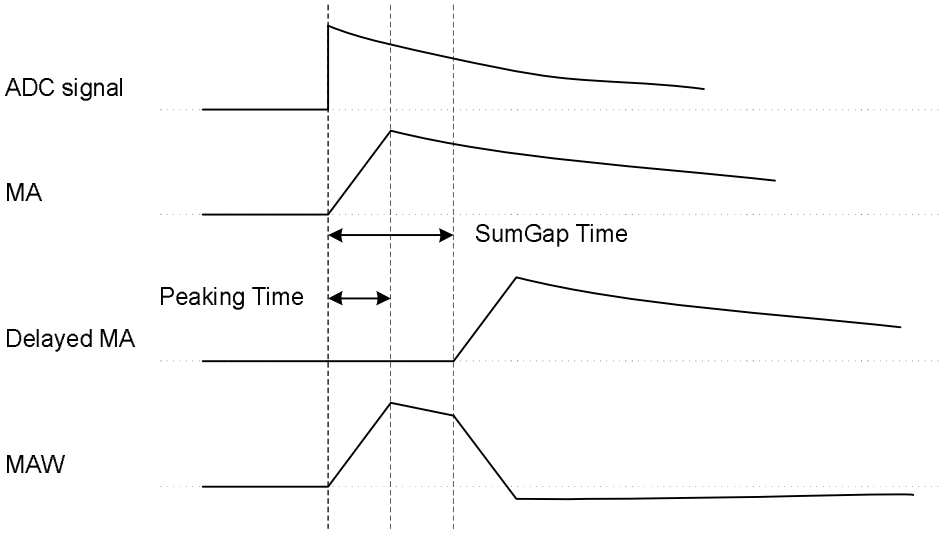
Trigger: trapezoidal FIR Filter

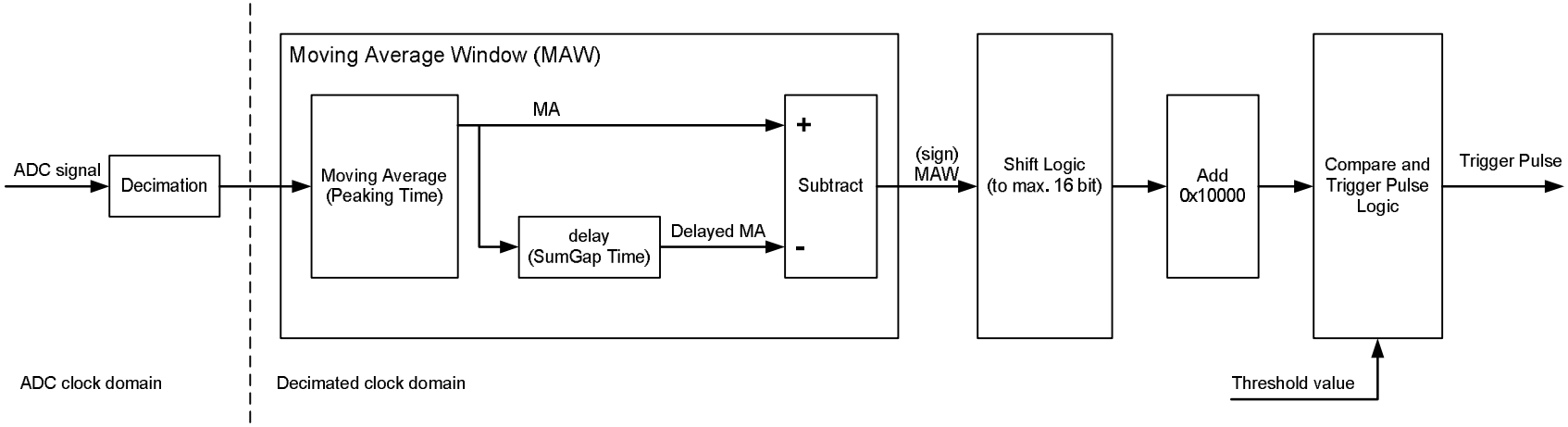
- A trapezoidal FIR filter is implemented for each ADC Channel to generate a trigger signal.

Features for each ADC channel:

- Programmable Peaking Time (max. 510 Clocks)
- Programmable Gap Time (max. 510 Clocks)
- Programmable Trigger Threshold
- Programmable CFD Mode
- Programmable Trigger Mode (GT,Disable)

Example from SIS3302

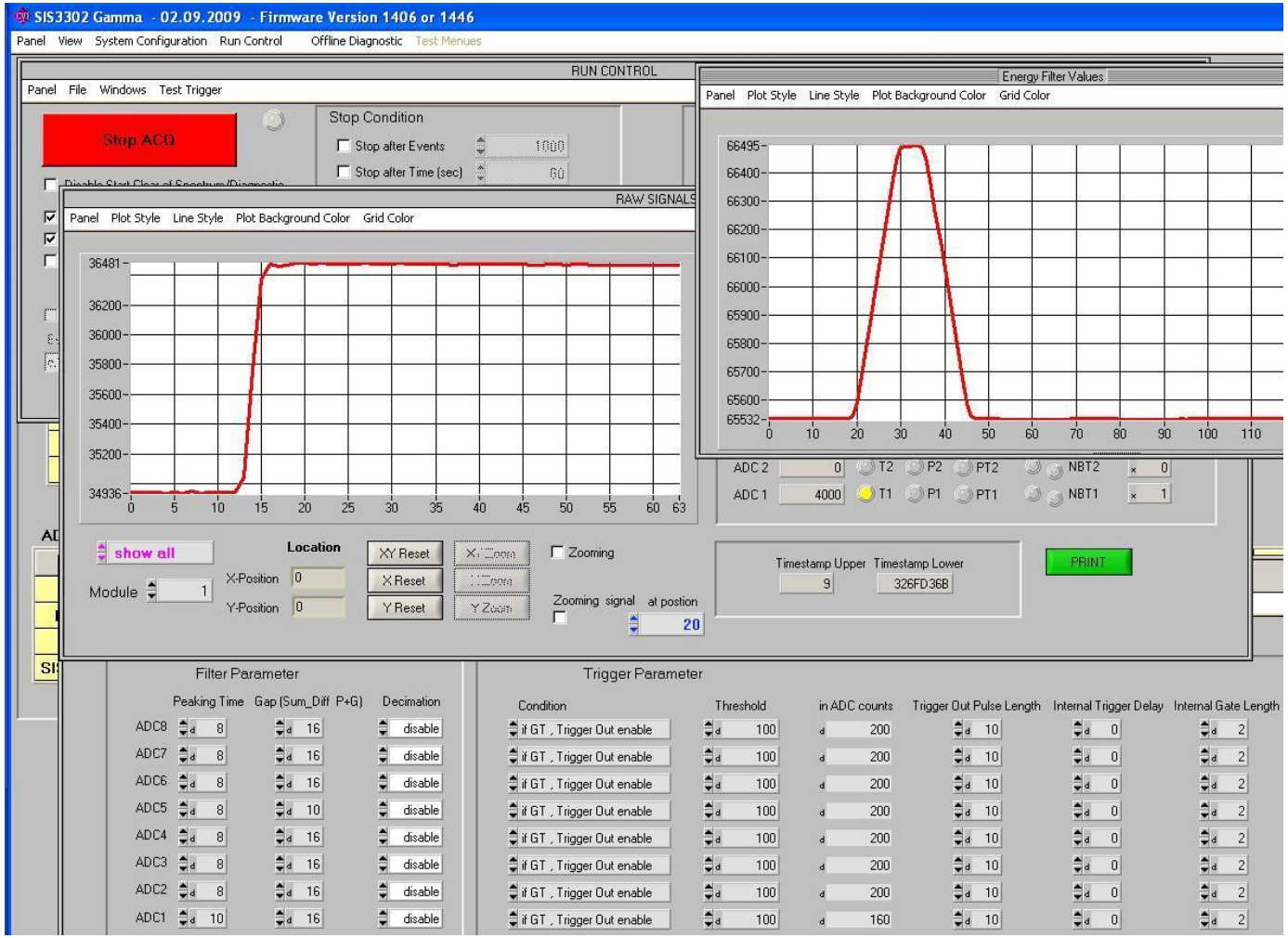




Explanation:

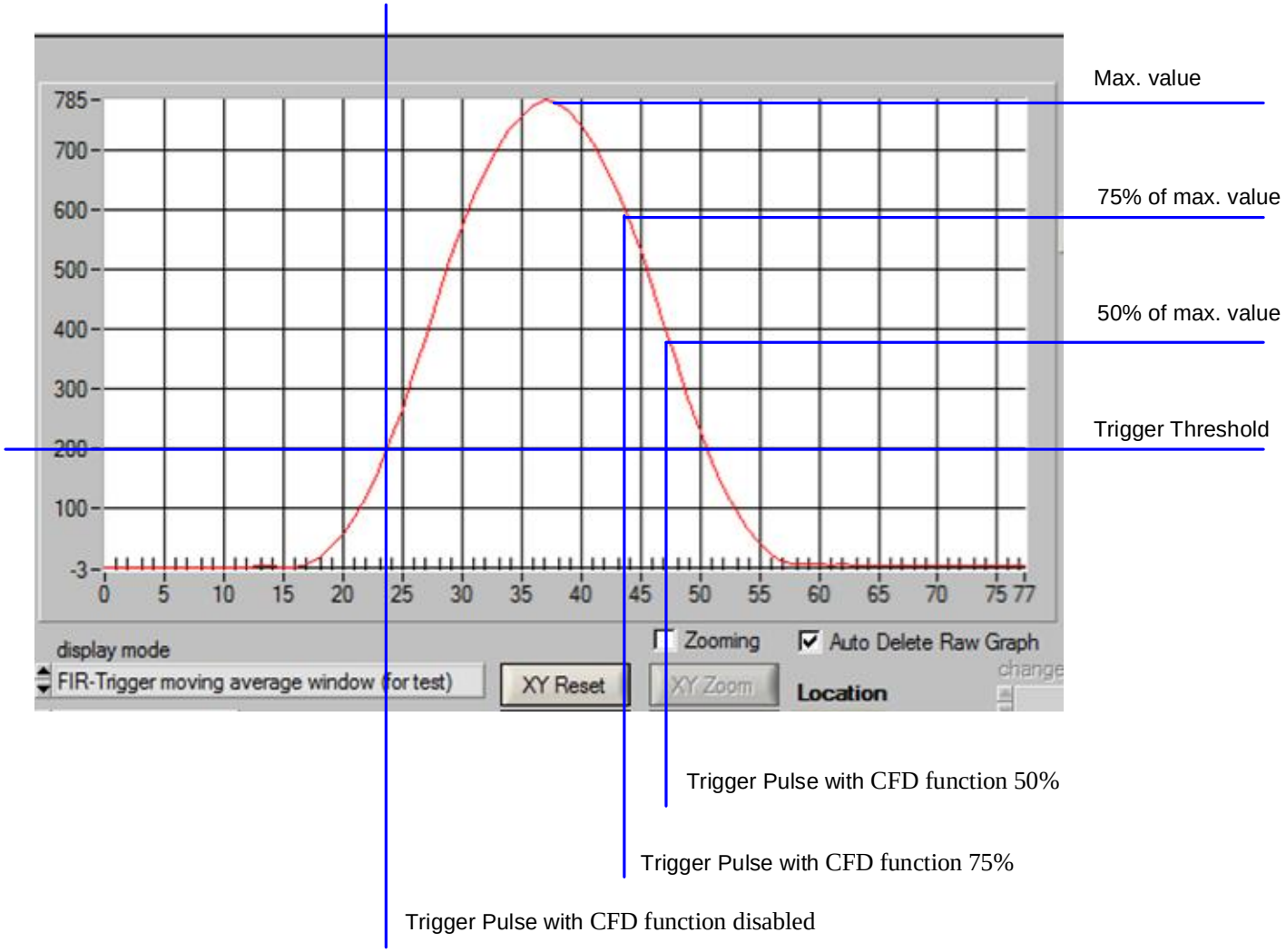
- •MAW: moving average window
- •MA: moving average
- •Decimation: decreasing the clock rate
- •Peaking Time: the length of the MA for moving average unit
- •SumGap Time: the differentiation time of the mowing window average unit

Example from SIS3302

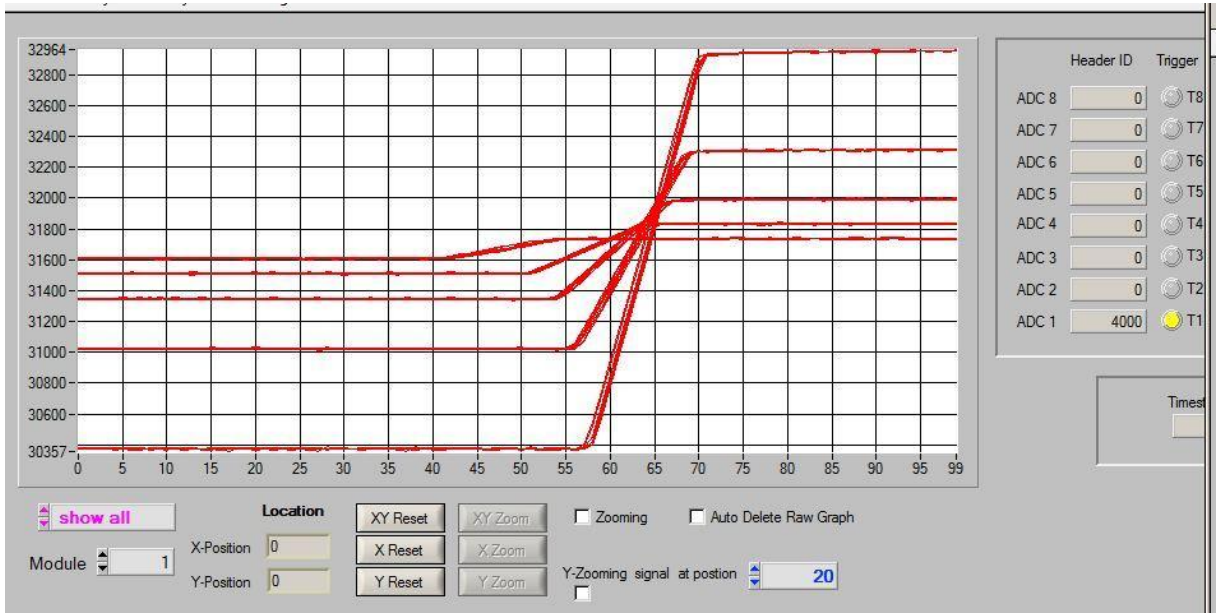


SIS3302 example: CFD Trigger

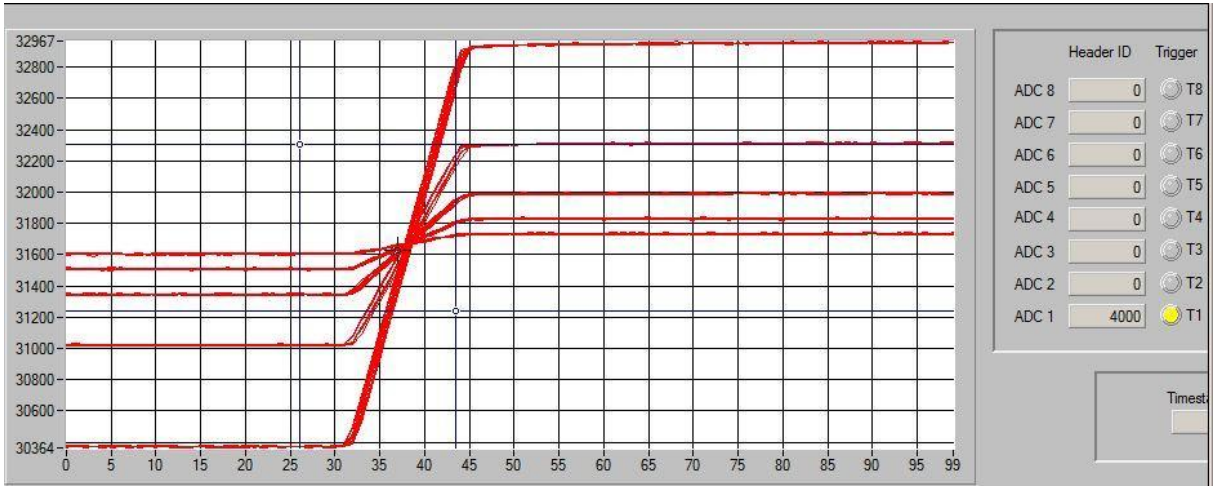
P = 10, G = 10 (sumG = 20)
Signal rise time 100ns



SIS3302 example: CFD Trigger disabled



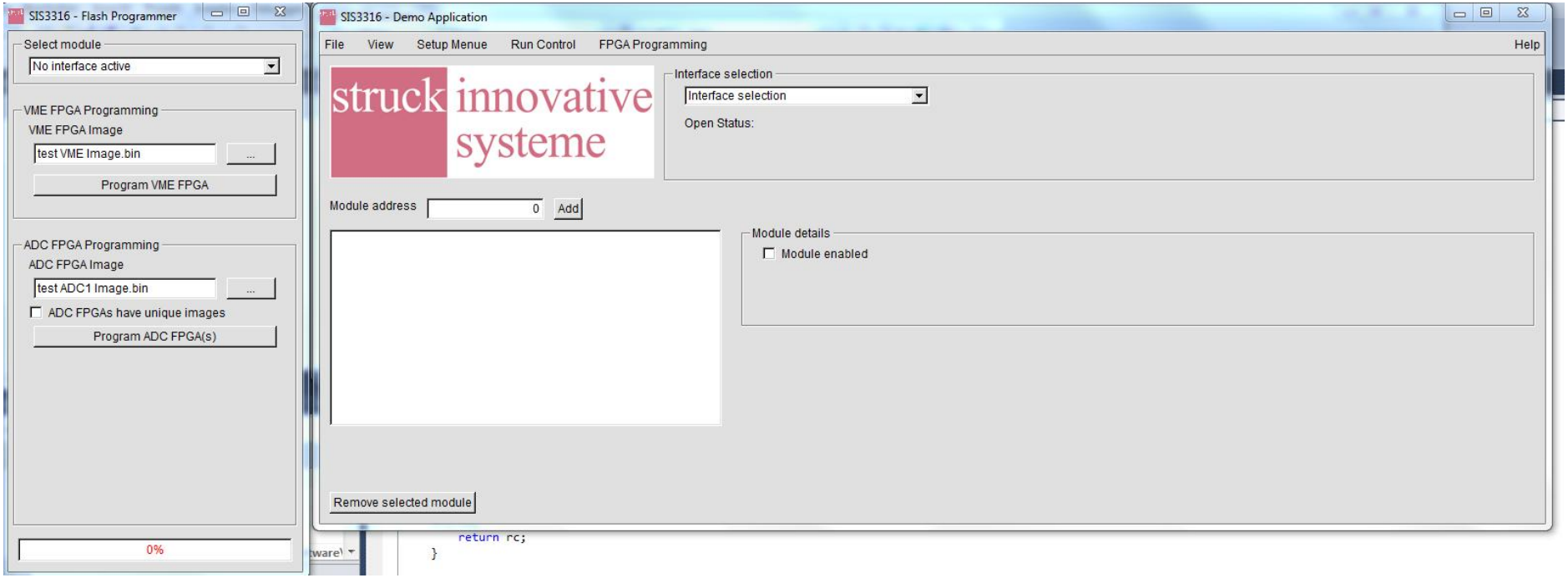
SIS3302 example: CFD Trigger enabled



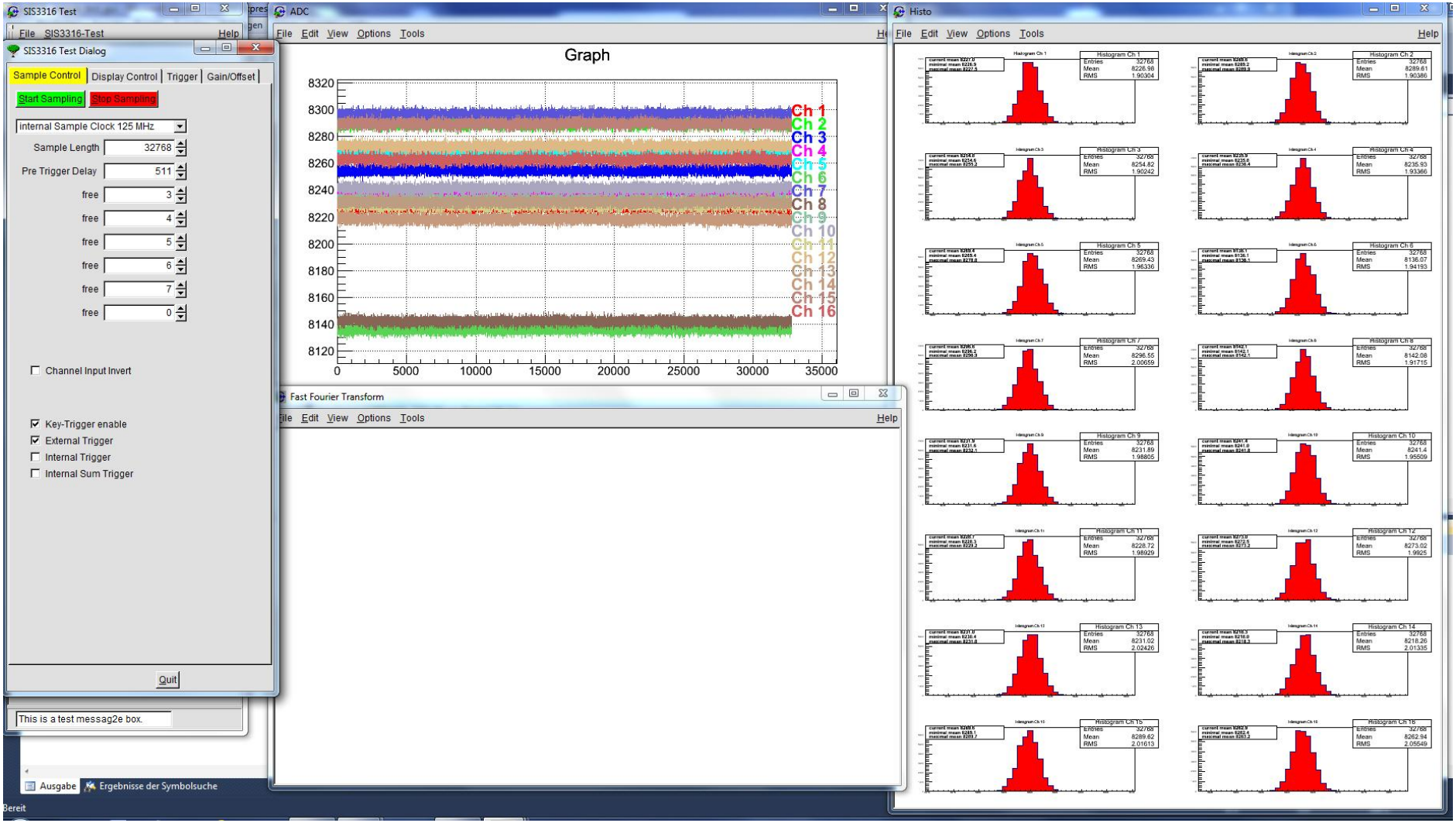
Status of ADC FPGA Implementation 25-08-2012

To be defined

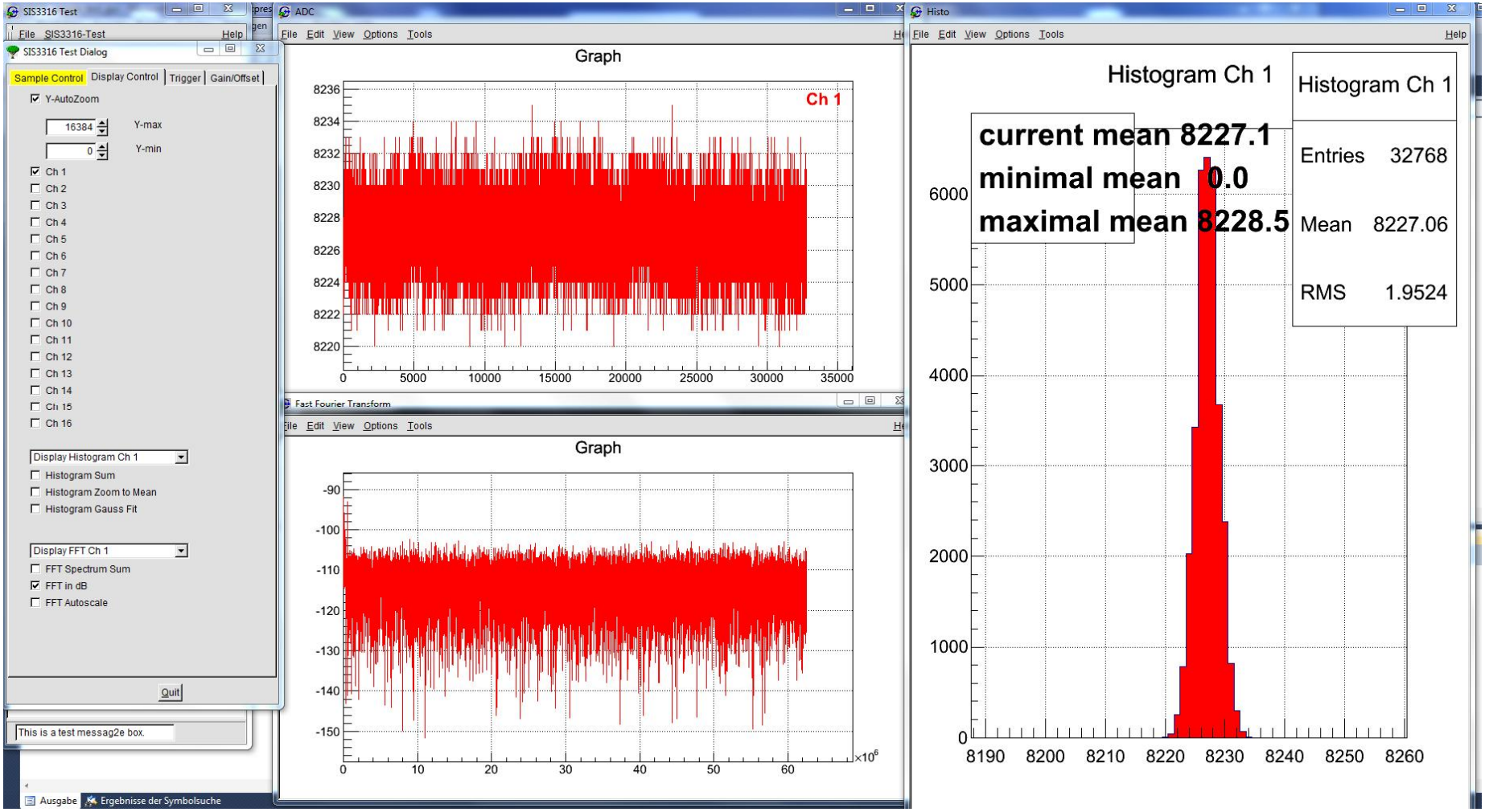
SIS3316 FPGA Flash Programmer (use Cern-Root)



SIS3316 Test GUI



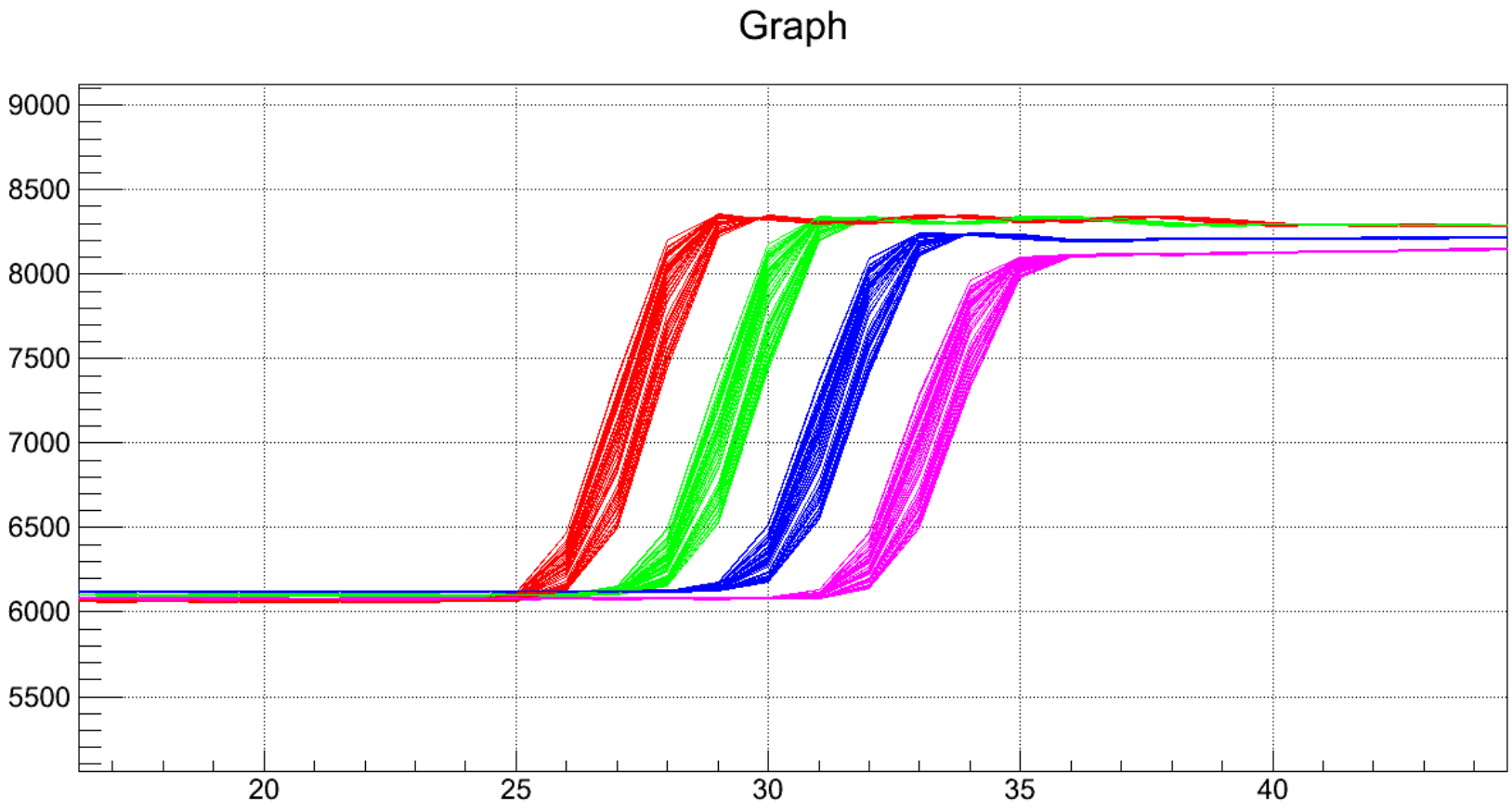
SIS3316 Test GUI



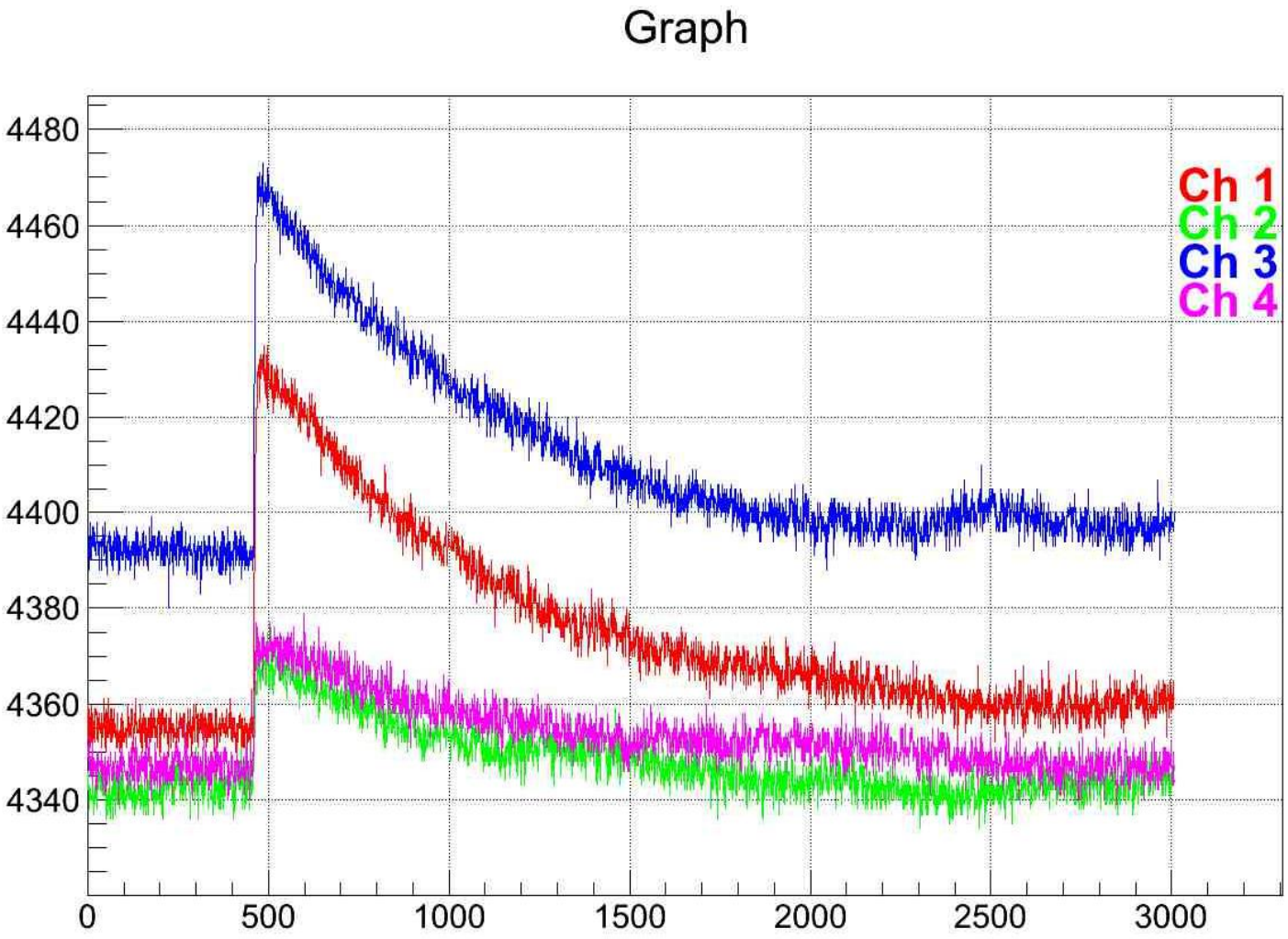
SIS3316 Test Application (CERN-Root)

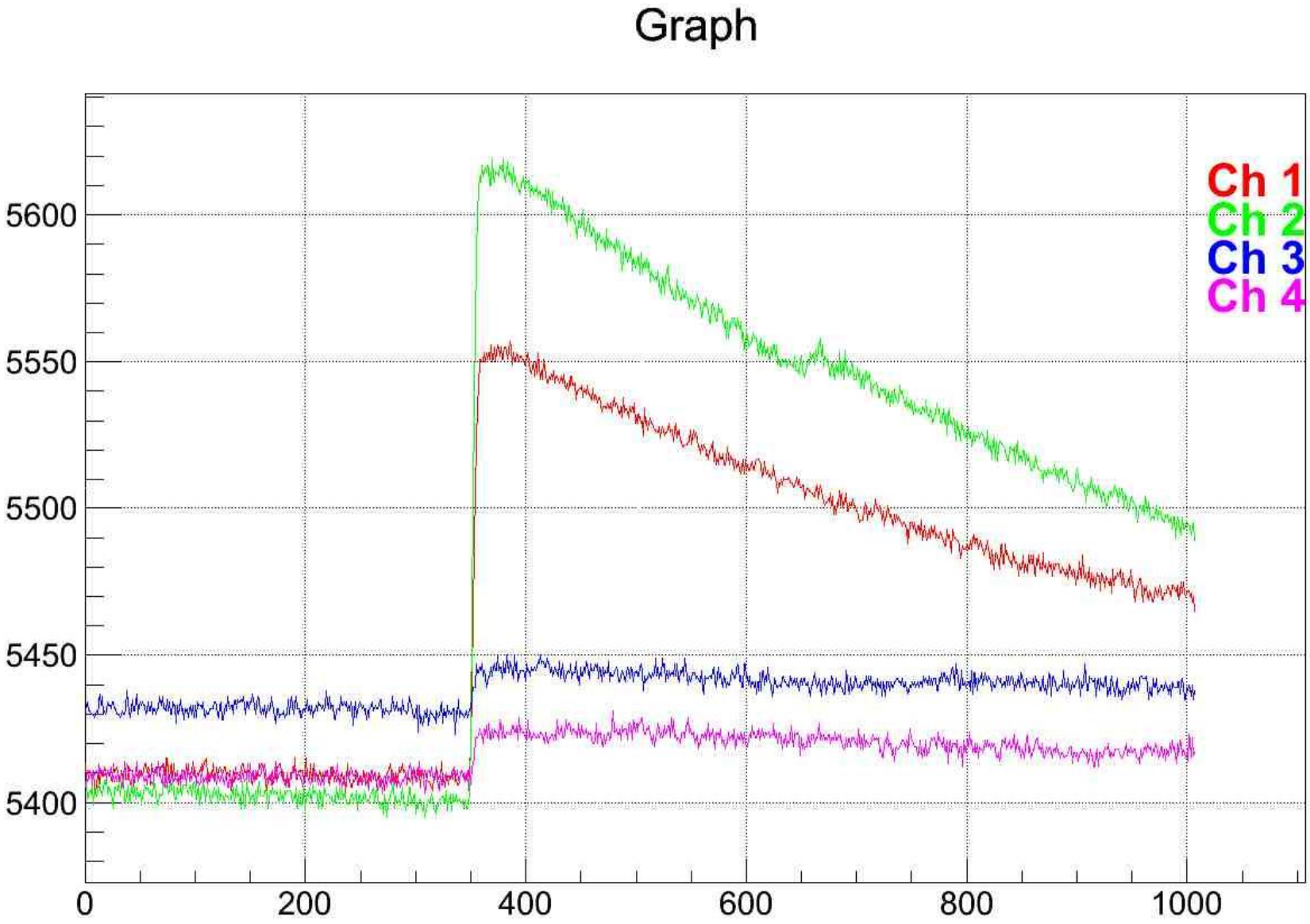
Shows Channel 1 to Channel 4:

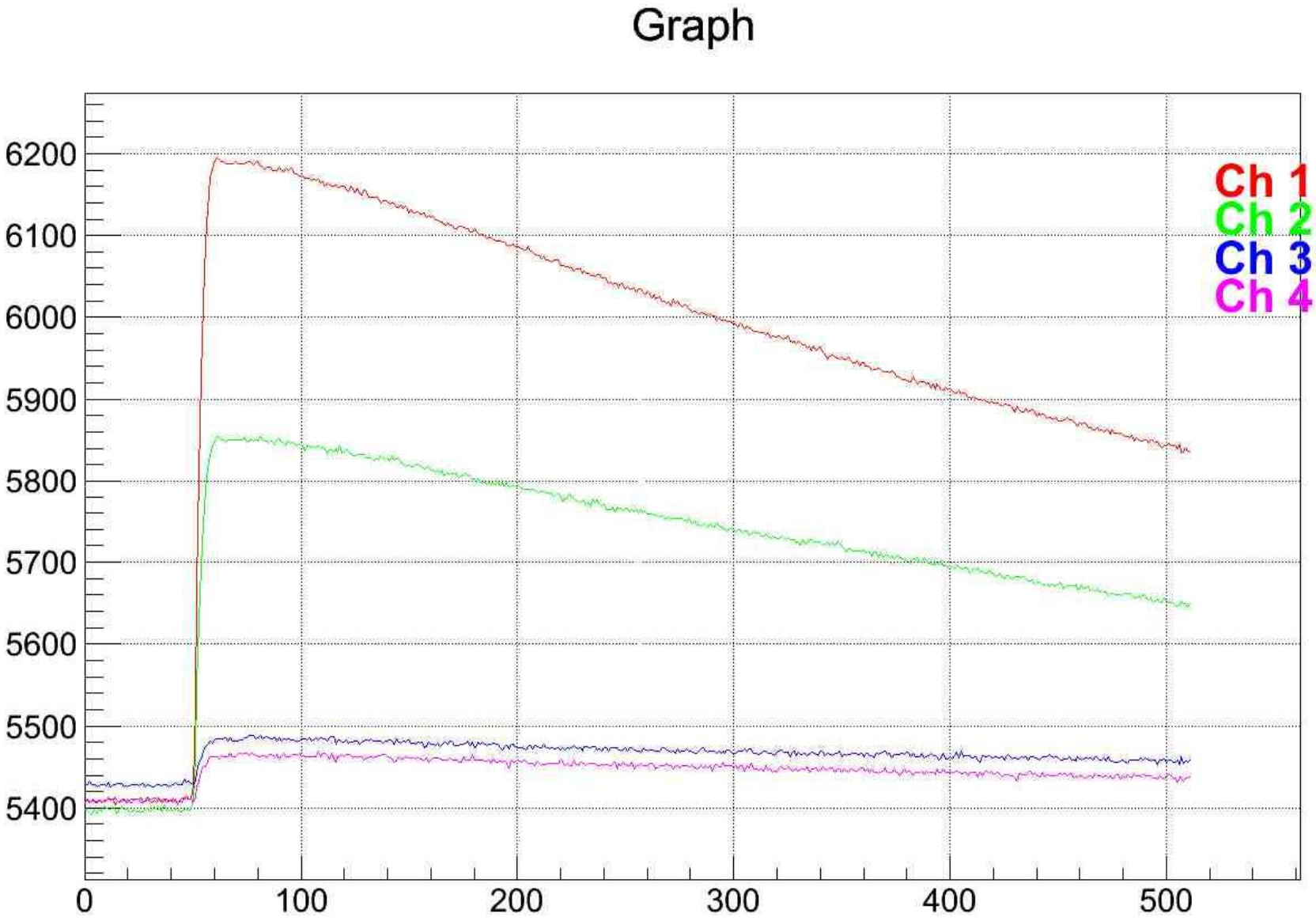
- Signal is delayed with 1.5 meter Lemo cables from ch 1 to ch 2, from ch 2 to ch 3 and from ch 3 to ch 4.



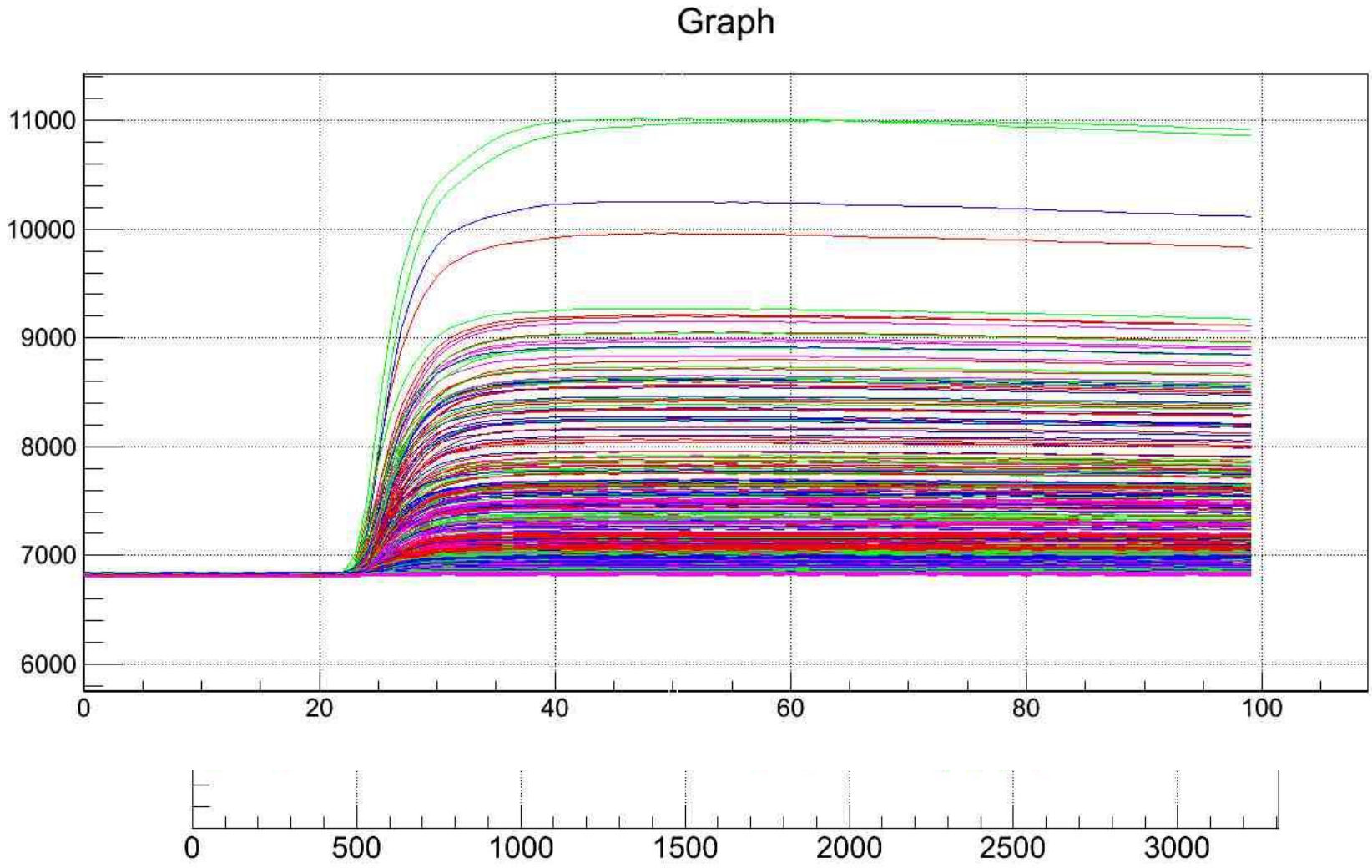
SIS3316 First Measurements at ORNL

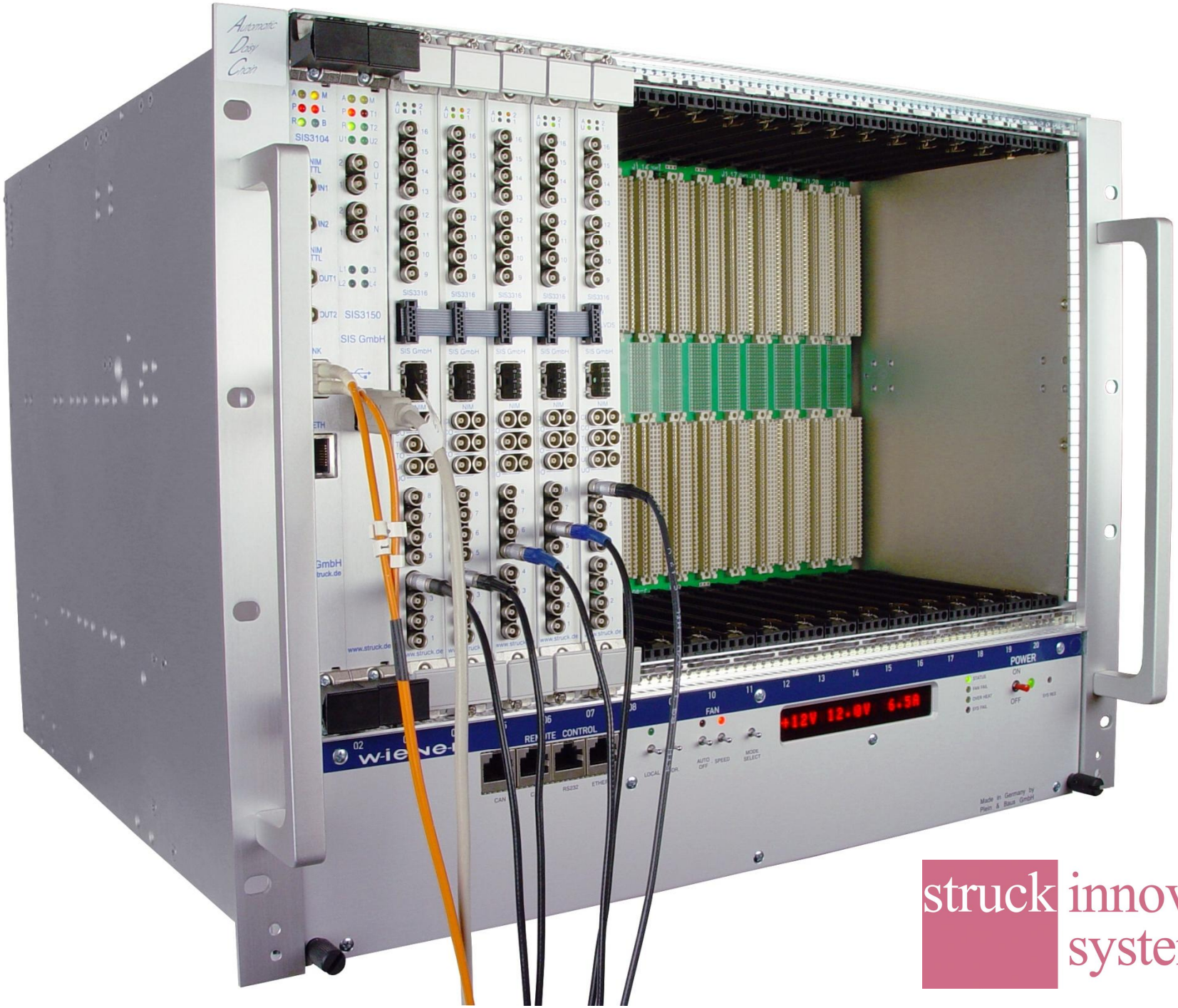



Graph
Ch 1
Ch 2
Ch 3
Ch 4
5600
5550
5500
5450
5400
0
200
400
600
800
1000


Graph
6200
6100
6000
5900
5800
5700
5600
5500
5400
0
100
200
300
400
500
Ch 1
Ch 2
Ch 3
Ch 4

SIS3316 First Measurements at ORNL





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