

SIS3300/3301 JTAG Firmware Upgrade Instructions

SIS GmbH
Harksheider Str. 102A
22399 Hamburg
Germany

Phone: ++49 (0) 40 60 87 305 0
Fax: ++49 (0) 40 60 87 305 20

email: info@struck.de
<http://www.struck.de>

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Revision Table:

Revision	Date	Modification
0.10	18.04.02	Generation
1.00	30.04.02	First official release
1.10	12.09.02	SIS3301 V2 and watchdog disable J190
1.20	03.11.05	Webpack/impact no longer on SIS CDROM → download from Xilinx web site
1.21	26.07.11	Bug fix in watchdog disable J190 Note: no update of outdated Impact screenshots and download information

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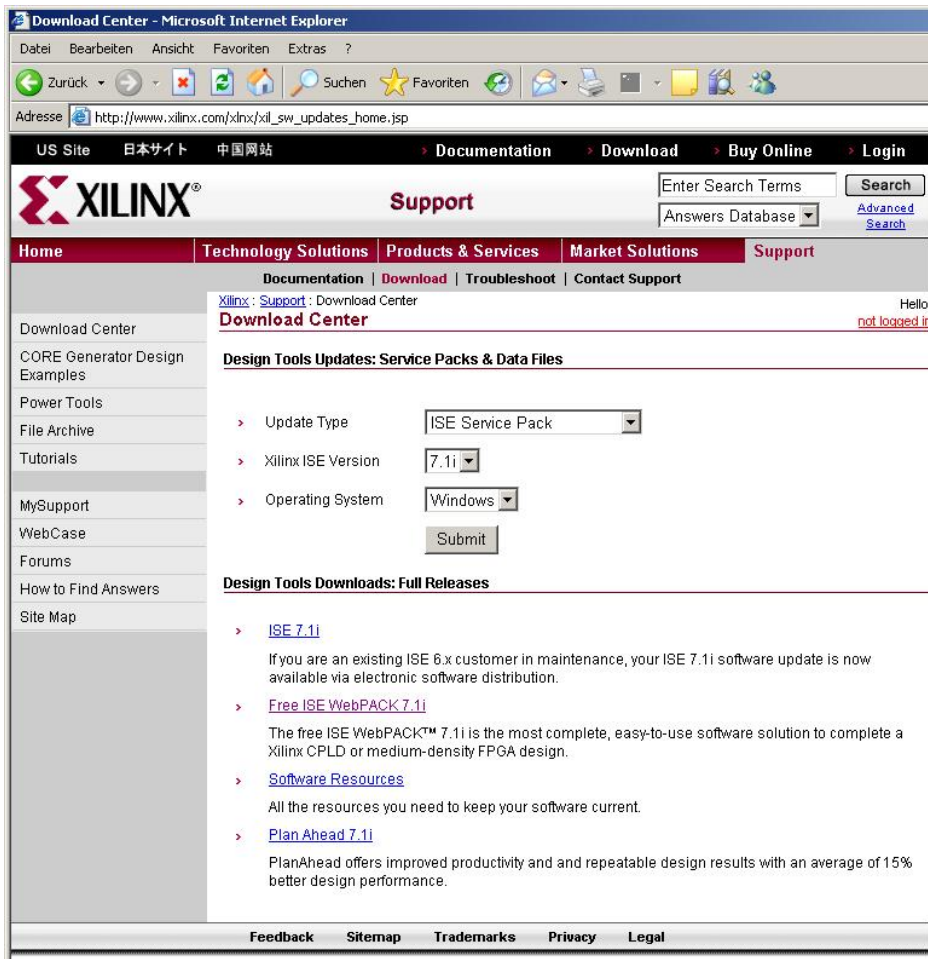
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2 Introduction

This document describes the firmware upgrade procedure of the SIS3300 and SIS3301 VME FADC cards via the JTAG port. The procedure was tested with a laptop under Windows 2000 and a Xilinx parallel port JTAG programming cable (i.e. HW-JTAG-PC).

3 Installation of iMPACT software

The iMPACT software is part of the ISE WebPACK, which can be downloaded from www.xilinx.com after creating/login onto a Xilinx account. You will find the free ISE WebPACK x.yi in the support download area as illustrated (for 7.1.i) below.



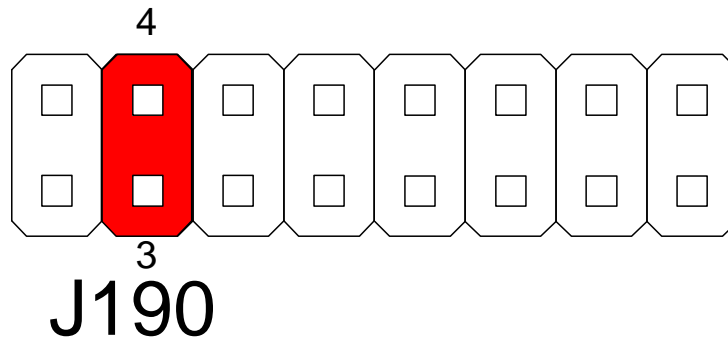
can be found on the

After installation you should have iMPACT on your PC as shown below. The iMPACT program is used to install the firmware over JTAG.



4 Watchdog disable

The watchdog has to be disabled before firmware download to avoid reset pulses from onboard watchdog logic during the download process. This is especially essential on cards with no intact firmware. The watchdog is disabled by disconnecting the link between Pins 3 and 4 on jumper array J190



Put the jumper back in place after the download procedure is finished.

5 JTAG connection

Connect the JTAG cable to the parallel port and to the SIS3330x . The JTAG connector and its pinout are illustrated below.

Start the software by double clicking the Icon on the desktop.

5.1 SIS3300/3301 JTAG connector

A photograph with the JTAG connector of the SIS330x is shown below.



5.2 SIS3300/3301 JTAG connector pinout

Pinning of SIS330x JTAG connector (XILINX_JTAG):

Pin	Pin designator
1	VCC
2	GND
3	nc
4	TCK
5	nc
6	TDO
7	TDI
8	nc
9	TMS

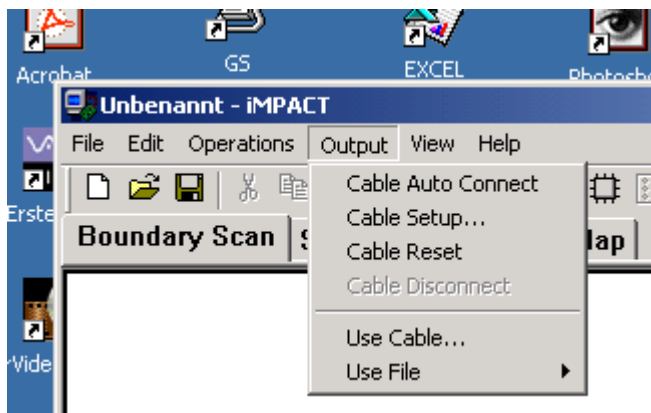
6 SIS330x firmware upgrade (below SIS3301 V2)

With printed circuit board revision SIS3301 V2 the JTAG chain was reduced to the serial PROMs. The firmware download description for boards at this revision level can be found in section 7

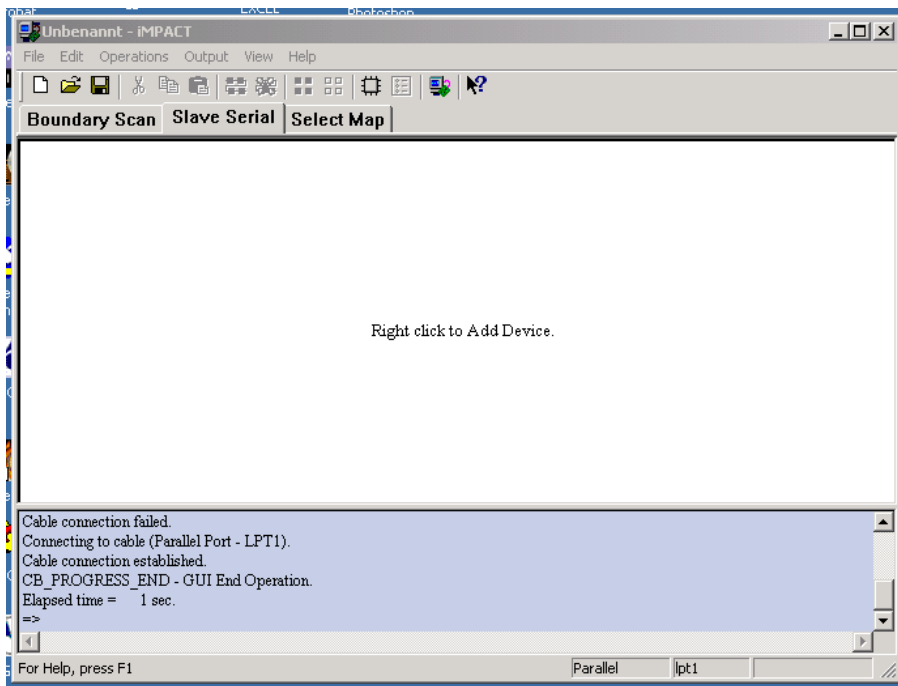
6.1 Establish Cable Connection

First you will have to establish a connection to your computers port (LPT1 in the example below).

At first startup you may have to select a connection, you may want to use Cable Auto Connect to do so.



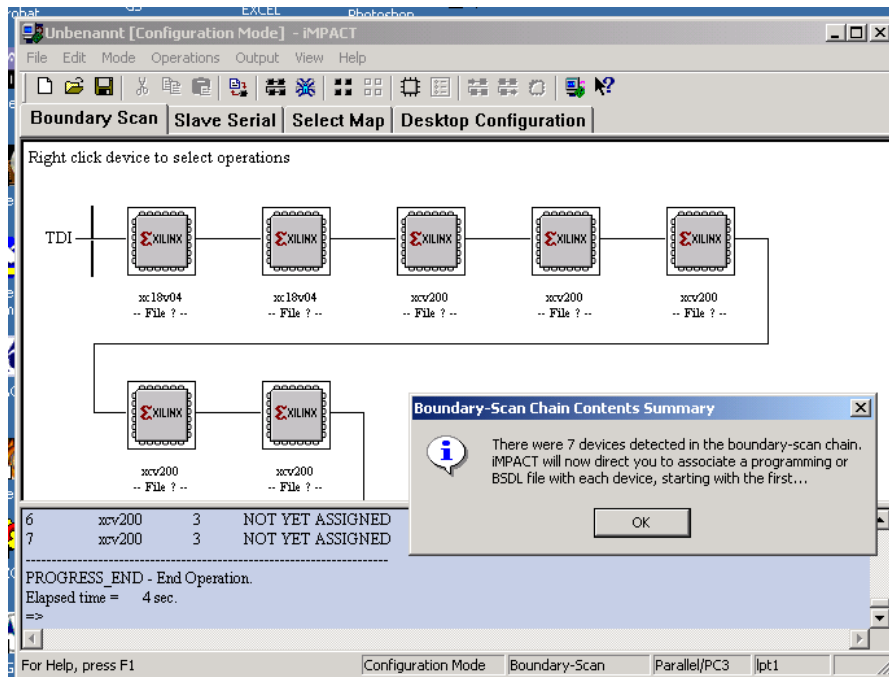
Once you have a proper connection established your screen will look like below.



6.2 Initialize chain

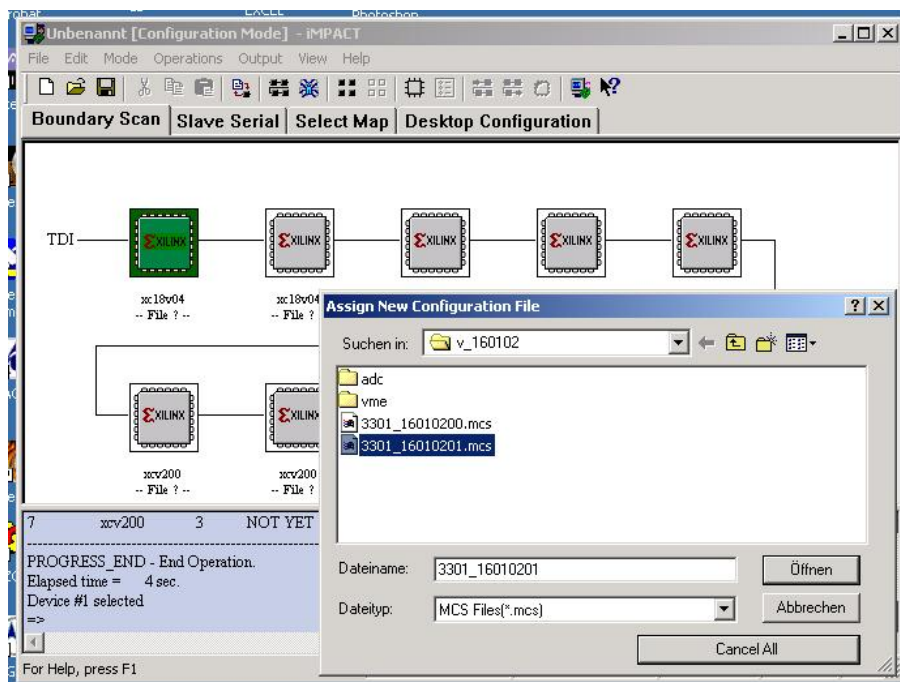
In this step the hardware will try to detect/initialize the JTAG devices in the chain. In the case of the SIS330x two serial PROMs (XC18V04) and 5 Spartan 2 FPGAs (reported as XCV200 Virtex FPGAs) have to be detected.

Note: the SIS330x will have to be under VME power for programming



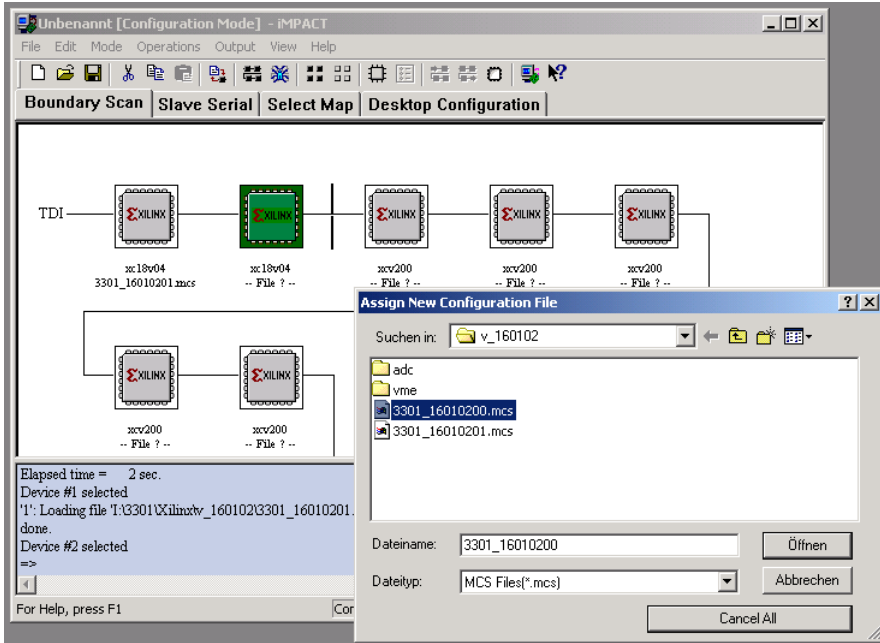
6.3 Select 1st device and programming file

The only devices that will be programmed are the two XC18V04 serial PROMs. Select the first device by double clicking on it. Chose the *.mcs file with the trailing 1 in the file name.



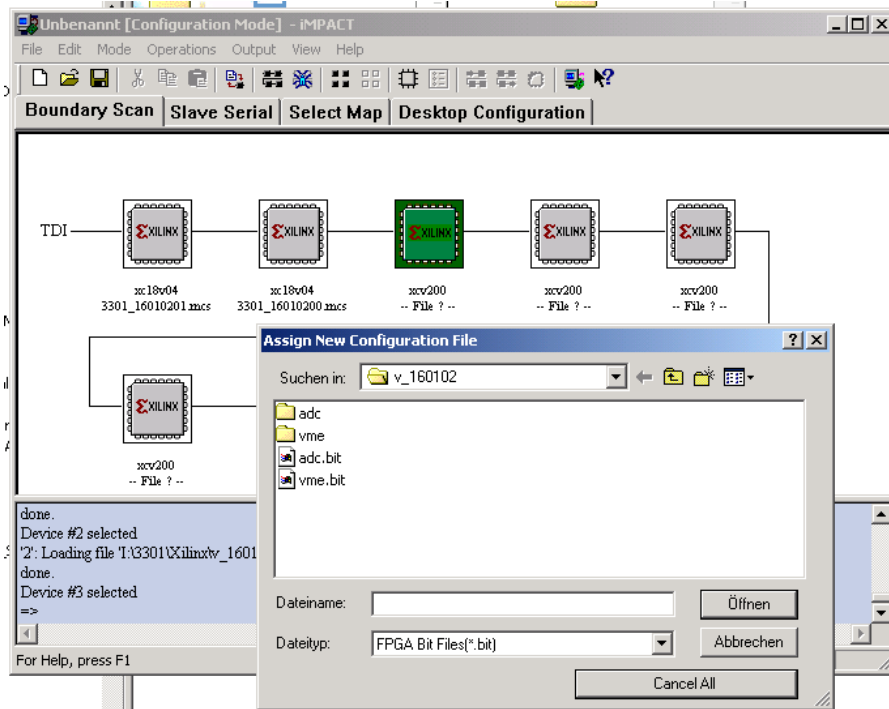
6.4 Select 2nd device and programming file

Select the programming files with the File pulldown. The first device is loaded with the file with the trailing 1 in the filename, the second is loaded with the file with the trailing 0 in the file name.



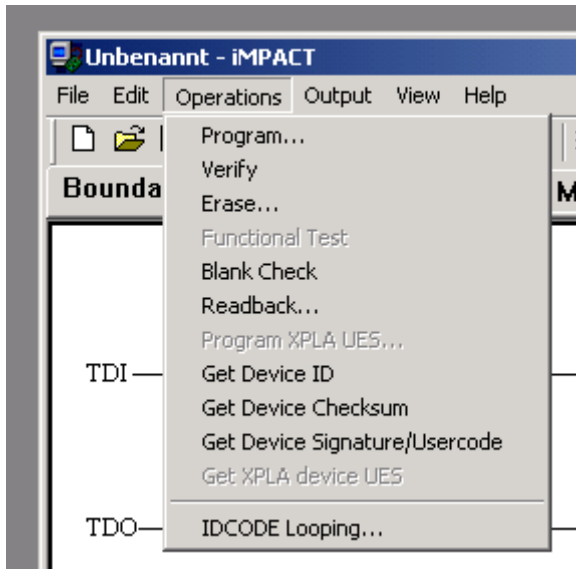
6.5 Cancel

Select Cancel All when prompted for the next configuration file (as we will want to programm the two serial PROMs only).

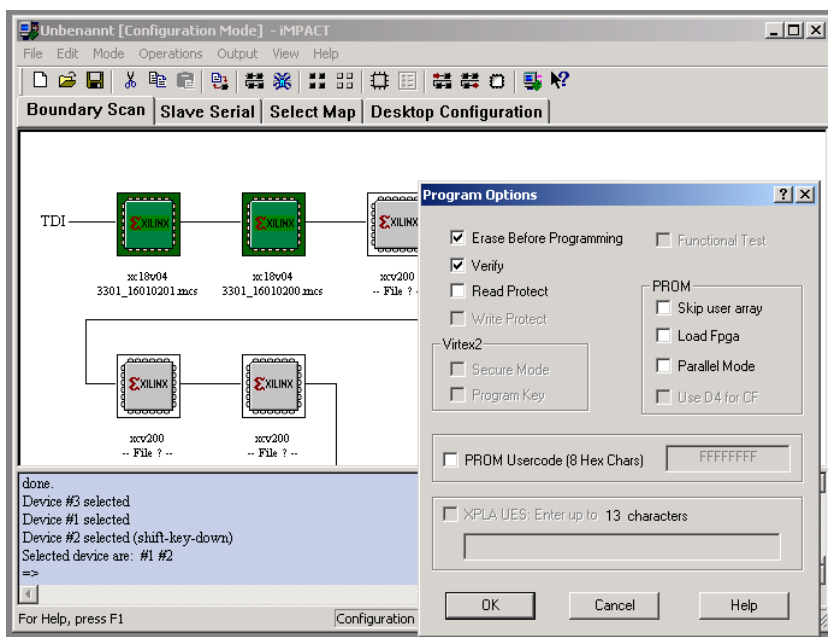


6.6 Program

Select the first two devices (i.e. the two XC18V04 PROMs) and program from the Operations pulldown.

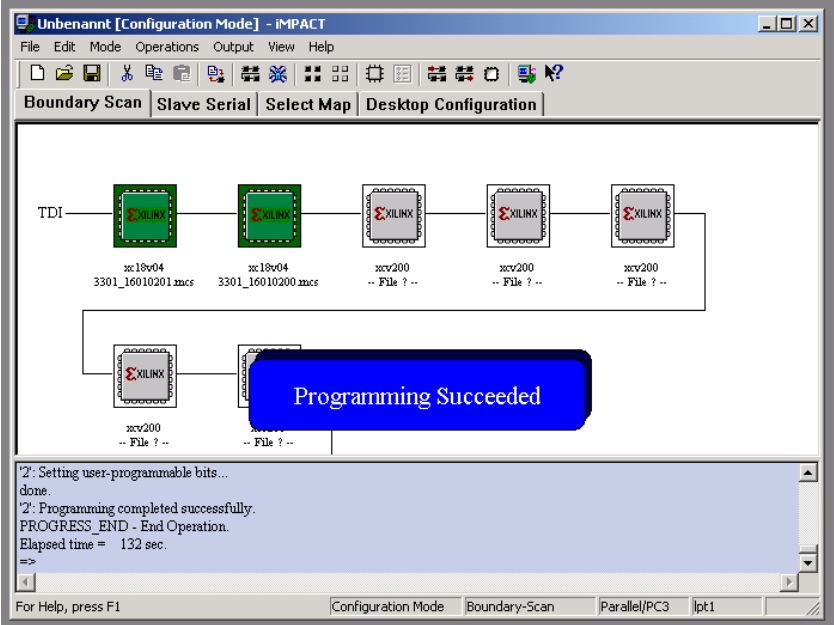


We will want to erase, program, verify and Load FPGA (a power cycle will be required after the firmware has been rolled in anyway).



6.7 Succeeded/completed

Upon successful completion the programming succeeded message will pop up for a while.

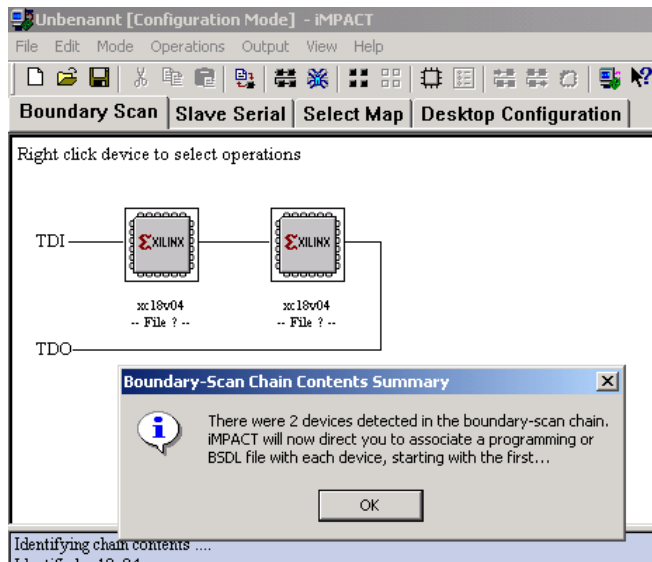


7 SIS330x firmware upgrade for SIS3301 V2

The procedure for the SIS3301 V2 is pretty much the same as the description for the earlier cards, but the JTAG chain is shorter.

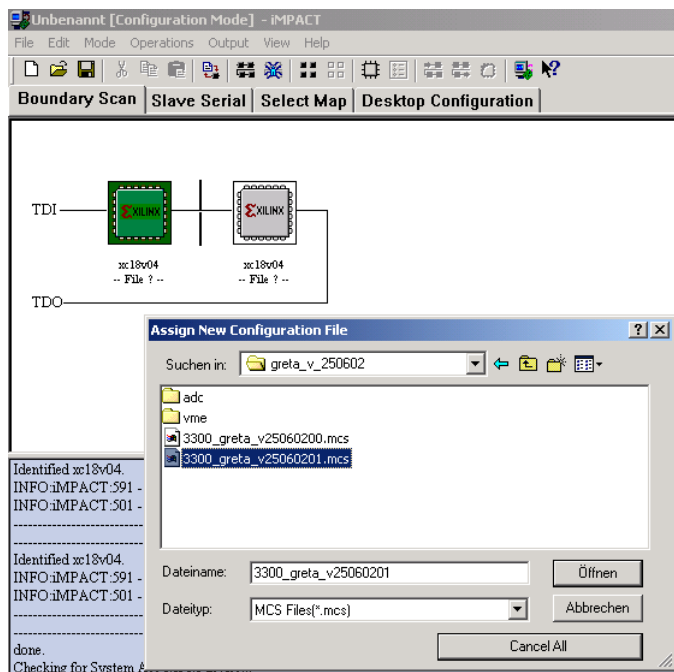
7.1 Initialize chain

Two XC18V04 serial Proms will be the only detected chips.

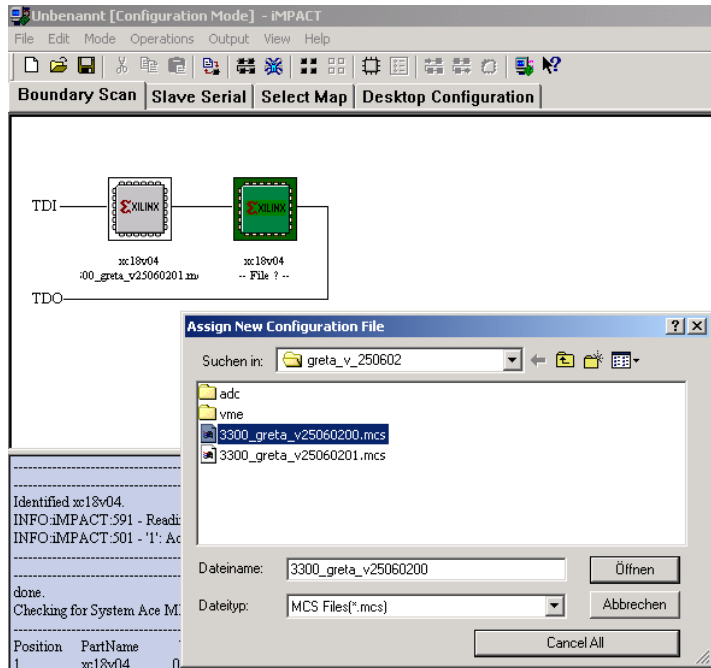


7.2 Select 1st programming file

The first serial PROM will get the file with trailing 1 in the filename.

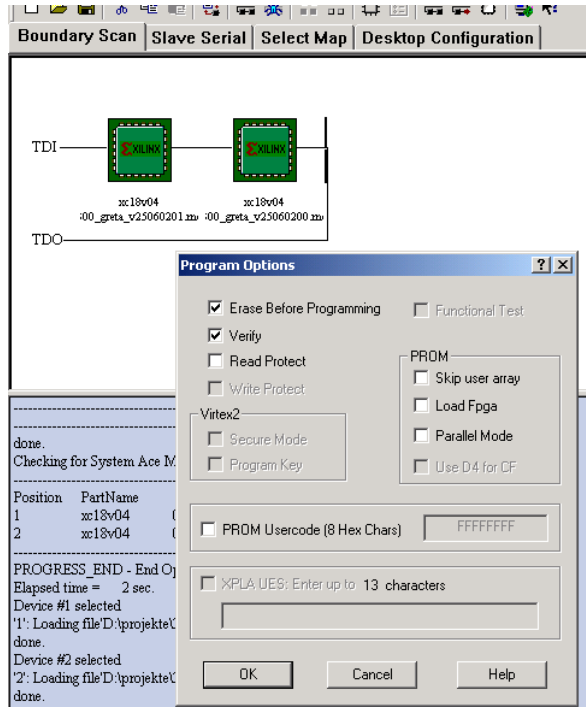


7.3 Select 2nd programming file



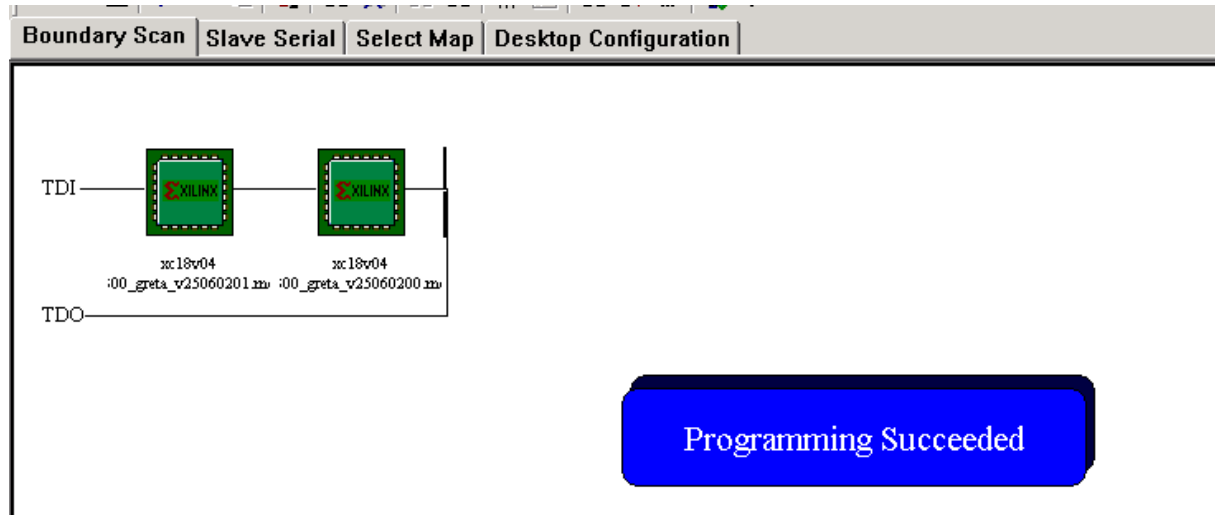
7.4 Program

Select the two chips for programming.



7.5 Completed

Upon successful completion you will get a screen like shown below for a minute.
Please note, that the complete process takes more than 2 minutes with a Parallel cable III.



Boundary Scan | Slave Serial | Select Map | Desktop Configuration

TDI — [XILINX] — [XILINX] — TDO

xc18v04 :00_greta_v25060201.m xc18v04 :00_greta_v25060200.m

Programming Succeeded

```
'2': Erasing device...
done.
'2': Erasure completed successfully.
'2': Putting device in ISP mode...
done.
'2': Programming device...
done.
'2': Putting device in ISP mode...
done.
'2': Putting device in ISP mode...
done.
'2': Verifying device...
done.
'2': Verification completed successfully.
'2': Calculated checksum matches expected checksum, 00214f353
'2': Setting user-programmable bits...
done.
'2': Programming completed successfully.
PROGRESS_END - End Operation.
Elapsed time = 134 sec.
```