SIS1100-CMC
PCI CMC Carrier

User Manual

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The SIS1100-CMC is manufactured by SIS under license of the ZEL department of the Research Center Jülich (FZ Jülich)

Revision Table:

Revision	Date	Modification
0.0	10.06.01	Generation
1.00	26.09.01	First official release

1 Table of contents

2 Introduction

The SIS1100-CMC PCI common mezzanine card (CMC) carrier board was developed at the research center Jülich in the framework of the joined SIS-Jülich PCI to VME interface development. The PCI side of the interface was split into two cards (i.e. the SIS1100-CMC carrier and the CMC Gigabit link board SIS1100-OPT) to allow for future reuse of the cards for other applications. It is expected, that a major part of the driver can be used for a variety of PCI-CMC designs.

This document describes the hardware design of the SIS1100-CMC board, for the integration of home made CMC cards the system developer will also have to deal with part of the non local bus FPGA firmware.

As we are aware, that no manual is perfect, we appreciate your feedback and will try to incorporate proposed changes and corrections as quickly as possible. The most recent version of this manual can be obtained by email from info@struck.de, the revision dates are online under http://www.struck.de/manuals.htm.

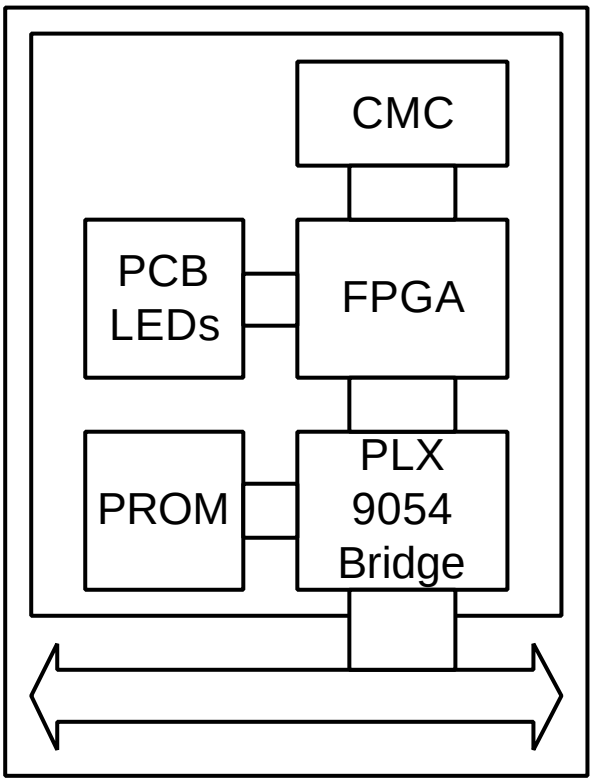
3 Technical Properties/Features

Find below a list of key features of the SIS1100-CMC.

? Single CMC site carrier board
? Standard PCI (32-bit, 33 MHz)
? PLX 9054 bus master PCI bridge chip
? JTAG interface
? serial boot PROM
? configuration PROM for PLX bridge
? single +5 V supply
? 3.3 V up to 7A generated by linear regulator
? 2.5 V up to 7A generated by linear regulator

3.1 Board Design

A block diagram of the card can be found below.



SIS1100-CMC block diagram

4 CMC connectors

4.1 CMC connector pin assignment

Pn1/Jn1				Pn2/Jn2			
Pin	Signal	Signal	Pin	Pin	Signal	Signal	Pin
1	Nc	Nc	2	1	Nc	Nc	2
3	GND	IO FIFO DQ0	4	3	Nc	Nc	4
5	Nc	IO FIFO DQ1	6	5	Nc	GND	6
7	Busmode1#	+5 V	8	7	GND	Nc	8
9	IO FIFO DQ2	IO FIFO DQ3	10	9	Nc	Nc	10
11	GND	IO FIFO DQ4	12	11	Busmode#2	+3.3 V	12
13	IO FIFO DQ5	GND	14	13		Busmode3#	14
15	GND	IO FIFO DQ6	16	15	+ 3.3 V	Busmode4#	16
17	IO FIFO DQ7	+5 V	18	17	Nc	Nc	18
19	+3.3 V	IO FIFO DQ8	20	19	Nc	Nc	20
21	IO FIFO DQ10	IO FIFO DQ9	22	21	GND	Nc	22
23	IO FIFO DQ11	GND	24	23	Nc	+3.3 V	24
25	GND	IO FIFO DQ12	26	25	Nc	Nc	26
27	IO FIFO DQ14	IO FIFO DQ13	28	27	+3.3 V	Nc	28
29	IO FIFO DQ15	+5 V	30	29	Nc	GND	30
31	+ 3.3 V	IO FIFO DQ16	32	31	Nc	Nc	32
33	IO FIFO DQ17	GND	34	33	GND	Nc	34
35	GND	IO FIFO DQ18	36	35	Nc	+3.3 V	36
37	IO FIFO DQ19	+5 V	38	37	GND	Nc	38
39	GND	IO FIFO DQ20	40	39	Nc	GND	40
41	IO FIFO DQ22	IO FIFO DQ21	42	41	+3.3 V	Nc	42
43	IO FIFO DQ23	GND	44	43	OUT_FIFO_WEN_L	GND	44
45	+ 3.3 V	IO FIFO DQ24	46	45	OUT_FIFO_WCLK	Nc	46
47	IO FIFO DQ25	IO FIFO DQ25	48	47	GND	Nc	48
49	IO FIFO DQ27	+5 V	50	49	OUT_FIFO_FFL	+3.3 V	50
51	GND	IO FIFO DQ28	52	51	IN_FIFO_OE_L	Nc	52
53	IO FIFO DQ30	IO FIFO DQ29	54	53	+3.3 V	Nc	54
55	IO FIFO DQ31	GND	56	55	IN_FIFO_REN_L	GND	56
57	+ 3.3 V	IO FIFO DQ32	58	57	IN_FIFO_RCLK	Nc	58
59	IO FIFO DQ34	IO FIFO DQ33	60	59	GND	Nc	60
61	IO FIFO DQ35	+5 V	62	61	IN_FIFO_EF_L	+3.3 V	62
63	GND	Nc	64	63	GND	Nc	64

Pn3/Jn3				Pn4/Jn4			
Pin	Signal	Signal	Pin	Pin	Signal	Signal	Pin
1	Nc	GND	2	1	+ 2.5 V	JTAG_TMS	2
3	GND	Nc	4	3	JTAG_CLK	JTAG_TDI	4
5	Nc	Nc	6	5	JTAG_TDO	GND	6
7	Nc	GND	8	7	GND	CMC_TO_OPT_CLK	8
9		Nc	10	9	Nc	CMC_RESET_L	10
11	OUT_FIFO_FLAG	Nc	12	11	Nc	+ 2.5 V	12
13	IN_FIFO_FLAG	GND	14	13	Nc	Nc	14
15	GND	Nc	16	15	+ 2.5 V	Nc	16
17	OPT_CTRL_15	Nc	18	17	Nc	GND	18
19	OPT_CTRL_14	GND	20	19	Nc	Nc	20
21	+ 3.3 V	Nc	22	21	GND	Nc	22
23	OPT_CTRL_13	Nc	24	23	Nc	+ 2.5 V	24
25	OPT_CTRL_12	GND	26	25	Nc	Nc	26
27	GND	Nc	28	27	+ 2.5 V	Nc	28
29	OPT_CTRL_11	Nc	30	29	Nc	GND	30
31	OPT_CTRL_10	GND	32	31	Nc	Nc	32
33	GND	Nc	34	33	GND	Nc	34
35	OPT_CTRL_9	Nc	36	35	Nc	+ 2.5 V	36
37	OPT_CTRL_8	GND	38	37	GND	Nc	38
39	+ 3.3 V	OPT_CTRL_23	40	39	Nc	GND	40
41	OPT_CTRL_7	OPT_CTRL_22	42	41	+ 2.5 V	Nc	42
43	OPT_CTRL_6	GND	44	43	Nc	GND	44
45	GND	OPT_CTRL_21	46	45	Nc	Nc	46
47	OPT_CTRL_5	OPT_CTRL_20	48	47	GND	Nc	48
49	OPT_CTRL_3	GND	50	49	Nc	+ 2.5 V	50
51	GND	OPT_CTRL_19	52	51	Nc	Nc	52
53	OPT_CTRL_4	OPT_CTRL_18	54	53	+ 2.5 V	Nc	54
55	OPT_CTRL_1	GND	56	55	Nc	GND	56
57	+ 3.3 V	OPT_CTRL_17	58	57	Nc	Nc	58
59	OPT_CTRL_2	OPT_CTRL_16	60	59	GND	Nc	60
61	OPT_CTRL_0	GND	62	61	Nc	+ 2.5 V	62
63	GND	Nc	64	63	GND	Nc	64

4.2 Jumper/Connector pin assignments

The SIS1100-CMC can be used without modification of the factory default jumper settings in standard applications. For in house firmware developments

4.2.1 B4/B5 JTAG

Firmware can be loaded into the serial PROM via the JTAG port.

B5:

Pin	Function
1	VCC
2	GND

B4:

Pin	Function
1	TCK
2	TDO
3	TDI
4	TMS

4.2.2 B8 JTAG chain

The JTAG chain can be routed to the CMC connector or closed on the SIS1100-CMC.

B8 closed	No CMC installed, close JTAG chain on SIS1100-CMC
B8 open	CMC installed, route JTAG chain over CMC

4.2.3 J1 XChecker

Pin	Function
1	VCC
2	GND
3	NC
4	CCLK
5	DIP
6	DIN
7	Program
8	Init

4.2.4 B1-B3 (M1-M3) Master serial mode

Please refer to the corresponding Xilinx docuementation

Note: Pin1 of a given jumper jumper array can be identified by the square pad

4.3 CMC Connector type

The used connectors are in accordance with xxxx (ref), spare connectors or connectors for your own CMC designs are available through SIS or a distributor of your choice.

Connector on SIS1100-CMC carrier board	
AMP120521-1	
Mating connector on CMC for 10 mm board to board spacing	
AMP120527-1	

Note: Parts from Molex can be used as compatible replacements as long as stacking height issues are taken care of. Please refer to the corresponding data sheets for details. (

5 LEDs

The SIS1100-CMC has 4 red printed circuit mounted SMD LEDs to visualise part of the units status. The function of the LEDs may depend on the firmware implementation, the table below lists their function in the base design of the SIS1100-CMC.

LED name	Function in base design
L11	
L12	
L13	
L14	

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