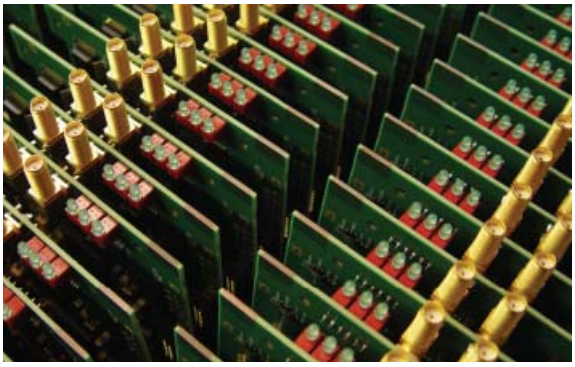
struck innovative systeme

Fall 2013/Spring 2014: Board Level Electronics Product Highlights

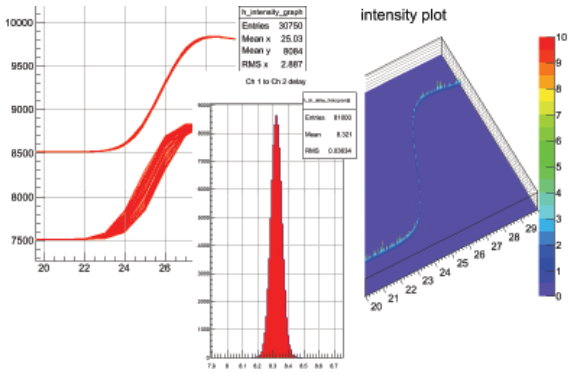
www.struck.de



2013 marks our 15th year in business.
We would like to take this opportunity to thank you for your patronage.
With the all new 16 channel SIS3316 VME digitizer and the Virtex 6 based SIS8300-L MTCA.4 digitizer we have exciting products for your application.

Our Product Range

- VME Interfaces/Bus Couplers/Digital I/O
- VME Digitizers/ADCs
- MTCA.4 Digitizers/ADCs
- USB2.0/3.0 and Ethernet Based Electronics
- PCI Express Cards
- Custom Designs



Application Examples

- Gamma Spectroscopy
- Accelerator Controls
- Synchrotron Radiation
- Neutron Scattering
- Plasma Physics
- Digitizer based TOF

Distributors

Australia
Scientific Devices Pty. Ltd.
Hamish Clark
118 Atkinson Street / PO Box 163
Oakleigh MDC, Vic 3166

Phone: ++61 3 9569 1366
Fax: ++61 3 9563 4728

email: hclark@scientific-devices.com.au

China
Beijing DAQ Technology Co., Ltd.
Chen Hua
B335, Forte Yuyuan Hotel,
Qinglongqiao, Haidian District
Beijing 100044, P.R. China

Phone: ++86 13 011236005
Fax: ++86 10 68924687

email: daqbeijing@vip.163.com

France
Acquitek
Philippe Vannier
1 bis rue Marcel Paul
91300 Massy, France

phone: ++33 1 60 13 52 73
Fax: ++33 1 60 13 03 68

email: philippe.vannier@acquitek.com

Struck
Distributor
Web Page

India
AdvanceTech Controls Pvt. Ltd.
Pradim Kulkarni
507, sagar Tech Plaza, Saki Naka Junction,
Andheri Kurla Road
Andheri(East), Mumbai-400 072
Phone: ++91 22 66980434;
Fax: ++91 22 66980433

email: pradipk@advancetech.in

Italy (Agent)

Ing. Roberto Cottica
Via Grigna 22
20025 Legnano, MI, Italy

Phone: ++39 0331 454455
Fax: ++39 0331 454455

email: rocotti@tin.it

Japan
REPIC
Shigeru Morinaga
28-3 Kita Otsuka 1-chome
Toshima-ku, Tokyo 170-0004, Japan

Phone: ++81 33918 5326
Fax: ++81 33918 5712

email: sales@repic.co.jp

Korea
J-Tech, Inc.
J. D. Kim
Room #202, Semyeong BLDG.
224-2, Dongchung-1-Dong, Yeonsu-Ku,
Incheon 406-131, Korea

Phone: ++82 32 811 0883
Fax: ++82 32 811 0884

email: jindookim@netsgo.com

USA
Drivesoft LLC
Michael Doebelin
1655 Murfreesboro Rd., Suite A
Old Hickory, TN 37217

Phone: (615) 758 3718
Fax: (615) 758 3973

email: mdoebelin@drivesoft.com

Table of Contents

VME Interfaces/Bus Couplers

new

SIS3153 USB3.0 to VME Interface

The SIS3153 is the latest extension to our VME interface product line. It combines the ease of use and convenience of USB with transfer speeds known from optical interfaces to date only as long as the maximum 3m cable length is not a limitation for your application

SIS3153

Functionality

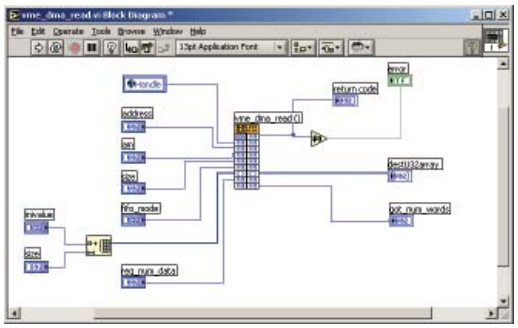
- Single width 6U VME master/system controller
- USB3.0/Superspeed USB functionality
- USB2.0 and USB1.1 compatibility
- 2 inputs/2outputs 00 LEMO, NIM/TTL level programmable
- SFP cage for optical or Ethernet link
- all relevant VME addressing modes up to 2eSST
- performant single cycle list array execution

Software Support

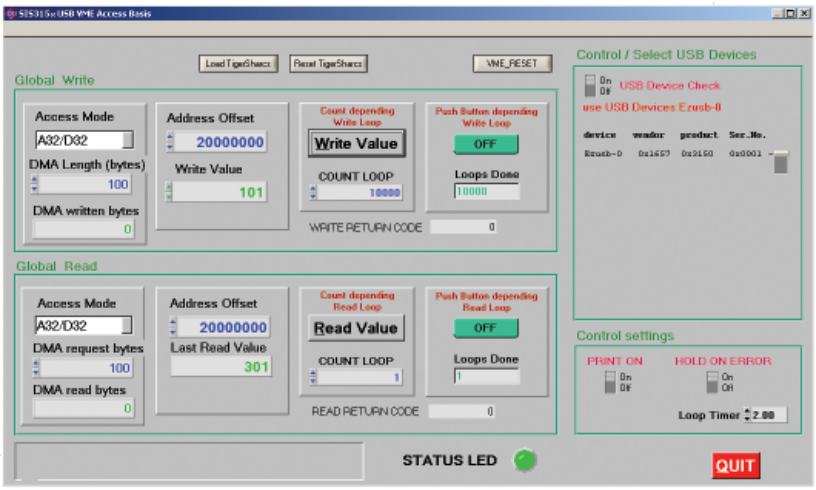
- Windows XP/7/8 and LINUX support
- Labwindows CVI/Labview support
- SIS3150 compatible calls

USB3.0 Transfer Speed

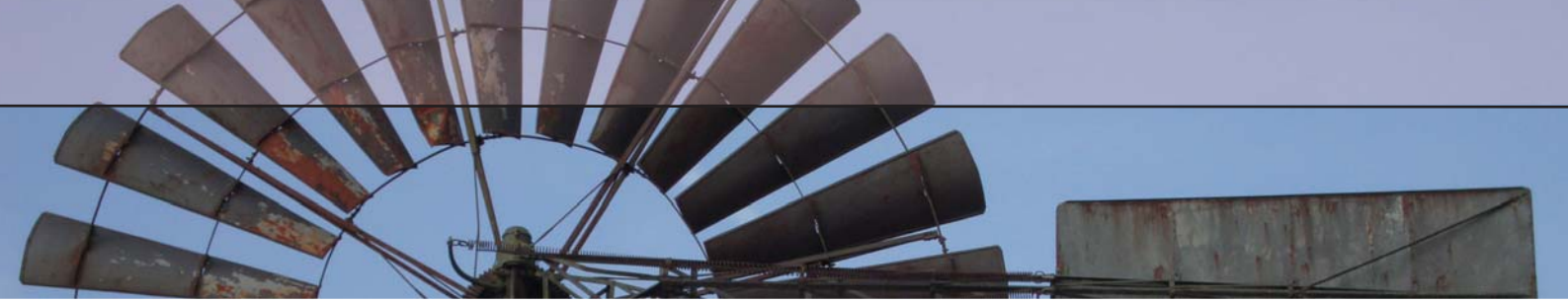
- 220 MByte/s block transfer
- 40 µs single read/write
- DMA speed single read/write list array execution



Labview Examples: Block Diagram of Block Read



Labwindows CVI Graphical User Interface of SIS315x base program



SIS1100/310x PCI/PCI Express/cPCI/AMC to VME Interface Family

This optical link based PCI/cPCI/PCIe to VME interface card family covers demanding VME data acquisition applications as well as the small laboratory test bench setup. VME readout speeds in excess of 160 MBytes/s are measured in a realistic SST VME master slave setup (SIS3350 ADC as VME slave e.g.). Windows and LINUX drivers in combination with example and user interface code facilitate the migration from other platforms and system integration.

SIS1100e/3104

Common Functionality

- 6U single slot form factor on VME side
- 128 entry mapping table
- VME master A16/A24/A32/D8/D16/D32/BLT32 MBLT64/2eMBLT64/2eSST
- block transfer address auto increment on/off (for FIFO reads)
- system controller function (to be disabled by jumper)
- up to 450 m link distance

Additional SIS3104 features

- SST implementation
- two front panel in- and outputs

Software Support

- Windows XP/Vista/7/8
- LINUX Kernel 2.6/3.0
- NI Labview/Labwindows
- VisualC++

Interface to	Interface Board	VME Board	Block Transfer Performance
PCI	SIS1100-uCMC/SIS1100-OPT	SIS3104	80 MByte/s
Compact PCI	SIS1100-cCMC/SIS1100-OPT	SIS3104	80 MByte/s
PCI Express	SIS1100-eCMC	SIS3104	80/160 MByte/s
µTCA/AMC	SIS8100	SIS3104	80/160 MByte/s
USB3.0	-	SIS3153	220 MByte/s
GBit Ethernet	-	SIS3153	to be implemented

VME Interface Overview

The SIS1100/3100 is a co-operative Forschungszentrum Jülich/Struck development.
SIS1100-uCMC and SIS1100-cCMC are produced under FZ-Jülich Lizenzvertrag 27

VME Digital I/O

SIS3820 Multi Purpose Scaler/Digital VME I/O Card

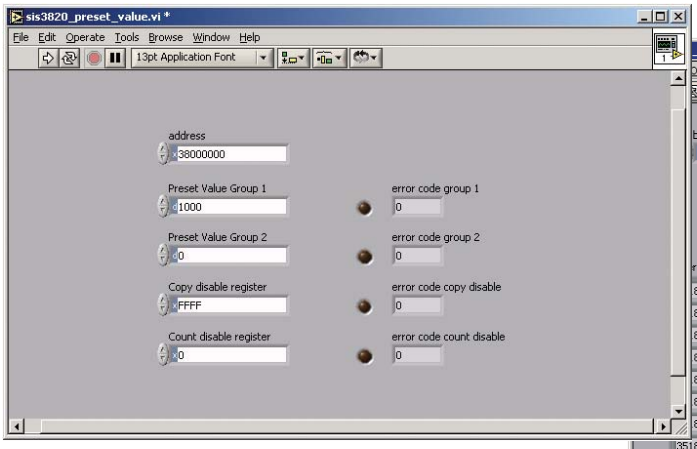
The module is a flexible FPGA based 6U VME board that allows for the implementation of a variety of digital I/O designs. Examples for off the shelf firmware designs are the 32 channel 200 MHz SIS3820-scaler and the 16 channel in/16 channel out SIS3820-latch designs.

SIS3820
LEMO and mixed

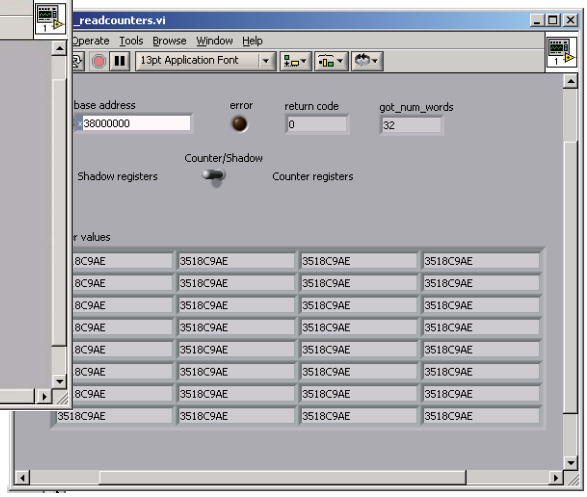
Functionality

- 4 control inputs
- 4 control outputs
- 32 input/output channels + 32 I/Os on P2
- 32 channel 200 MHz scaler/counter implementation
- on board histogramming functionality
- TTL/ECL/NIM/LVDS and other logic level options
- 64/512 MByte SDRAM options
- flat cable, coax. connector and mixed options
- in field firmware upgrade
- A32/D32/BLT32/MBLT64/2eVME
- 80 MBytes/s with SIS1100(e)/310x in 2e VME
- Windows and LINUX software support for SIS1100/310x interfaces

Design	Functionality
SIS3820	32 Channel Multi Purpose Scaler
SIS3820-Clock	Clock Distributor for Digitizers
SIS3820-3600	32-bit Latch w. Counter
SIS3820-3601	16 In/16 Out Register w. 4 Scalers and 4 Flipflops
SIS3820-1500	16 In/48 Out w. Pulse Generators
SIS3820 Firmware Implementations	



SIS3820 Preset Value Labview VI



SIS3820
Read counters
Labview VI
(in 25 MHz test
pulse mode)

SIS3820 Connector Options

Version	Control I/O	Channels 1-16	Channels 17-32
LEMO	LEMO	LEMO	LEMO
Flat Cable	Flat Cable	Flat Cable	Flat Cable
Mixed	LEMO	Flat Cable	Flat Cable
Mixed	LEMO	LEMO	Flat Cable
Mixed	Flat Cable	LEMO	Flat Cable
Mixed	LEMO	Differential LEMO*	Differential LEMO*

Table of SIS3820 Connector Options

* piggy card with 8 connectors

SIS98xx VME64x Transition Boards

SIS9820 Optical and TTL Output Card

The SIS3820 board has two times 16 I/O lines that are routed from the frontend FPGAs to the P2 connector. They can be accessed by means of VME64x transition cards. An example of a custom design for an accelerator control system is the SIS9820 board.

The SIS9820-V1 (shown to the right) features:
- DC/DC converters to supply +15/-15 V to external hardware
- two 15-pin DSUB connectors with 12 TTL outputs each
- 3 optical outputs with ST connectors

The SIS9820-V2 features:
- additional 4th optical output
- TTL LEMO outputs to monitor optical outputs

SIS9820

SIS9821 32 Channel Input Card

The SIS9821 board feeds 32 signals to the two times 16 I/O lines of the SIS3820 card. In combination with the corresponding firmware it expands the SIS3820 to a 64 channel scaler or 64-bit input register/latch.

The SIS9821 features:
- DC/DC converter to supply negative voltage for NIM/ECL configurations
- power LED
- TTL/ECL/NIM/LVDS and other logic level options
- flat cable, coax. connector and mixed options
- same configuration options as SIS3820 input channels

Feel free to inquire about custom SIS98xx designs

SIS9821

VME Digitizers

VME Digitizer Overview Table

Module	Sampling Speed	Channels	Resolution	Memory
SIS3305	5 GS/s	2	10-bit	512 MSample/channel
SIS3305	2.5 GS/s	4	10-bit	256 MSample/channel
SIS3305	1.25 GS/s	8	10-bit	128 MSample/channel
SIS3350	500 MS/s	4	12-bit	128 MSample/channel
SIS3316-250-14	250 MS/s	16	14-bit	64 MSample/channel
SIS3320-250	250 MS/s	8	12-bit	32 MSample/channel
SIS3316-125-16	125 MS/s	16	16-bit	64 MSample/channel
SIS3302	100 MS/s	8	16-bit	32 MSample/channel
SIS3302-4	100 MS/s	4	16-bit	32 MSample/channel

VME Digitizer Overview

Link to Struck Digitizer Overview Web Page

Typical Common Properties

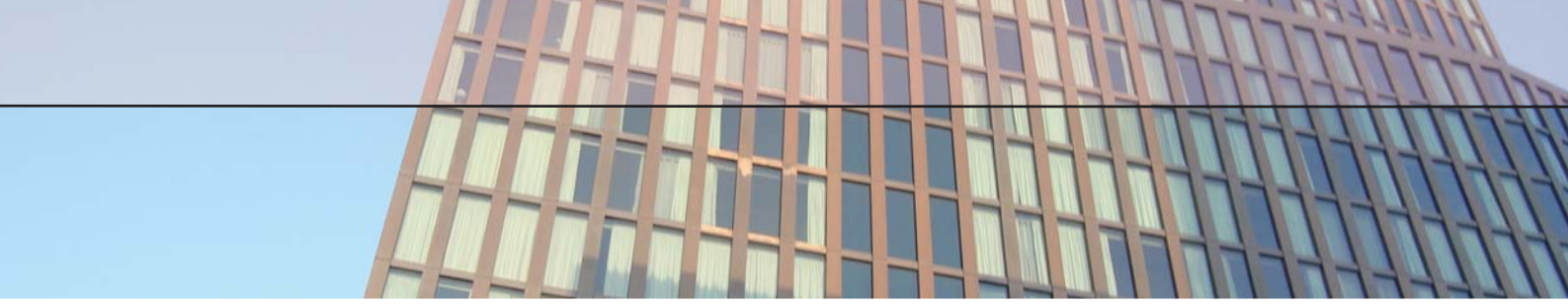
- Flexible input range configuration
- Single ended and differential inputs on 8 channel units up to 250 MS/s, single ended on all other boards
- Standard analog bandwidth up to Nyquist frequency, reduced or higher bandwidth on request

Firmware

Application specific firmware is available besides the oscilloscop like generic firmware where appropriate. Examples are Gamma, n/Gamma, Histogramming ADC and PSD readout.
For most units we do have IP firmware building blocks that can be used to base firmware extensions on. In the case of the SIS3302 the resulting project from a co-operation with the user is available on www.opencores.org.
Feel free to inquire about full custom firmware or firmware extensions to existing designs.

128 channel 1.25 GSPS 10-bit SIS3305 Digitizer system

80 channel 250 MSPS 14-bit SIS3316 Digitizer system with front panel bus



SIS3302 8 Channel 100 MS/s 16-bit VME Digitizer

The SIS3302 is our highest resolution digitizer. It embraces high dynamic range measurements as well as high resolution semiconductor spectroscopy and many other applications. A SIS3302 with Gamma firmware harnessing the Multi Channel Analyzer (MCA) implementation is perfectly suited to acquire spectra at synchrotron beamlines in conjunction with a SIS3820 in Multi Channel Scaler (MCS) mode of operation e.g..

SIS3302 and SIS3302-4

Functionality

- 4/8 channels with 16-bit resolution
- 1 - 100 MSamples/s per channel
- random clock mode for slower acquisition
- > 50 MHz analog bandwidth
- 32 MSamples/channel memory
- programmable offset (DACs)
- internal/external clock
- trigger input and output
- refer to the table below for available input configuration options
- flexible acquisition and readout features
- firmware discriminator
- A32/D32/BLT32/MBLT64/2eVME
- generic and application specific firmware designs (see table below)
- custom firmware development support
- in field JTAG and VME firmware* upgrade

Major/Minor Firmware Id.	Functionality
0x01 yy	8 Channel Generic Digitizer
0x14 0y	8 Channel Gamma with MCA
0x14 4y	4 Channel Gamma with MCA
0x15 0y	8 Channel Gamma, long filters
0x31 yy	8 Channel Neutron/Gamma

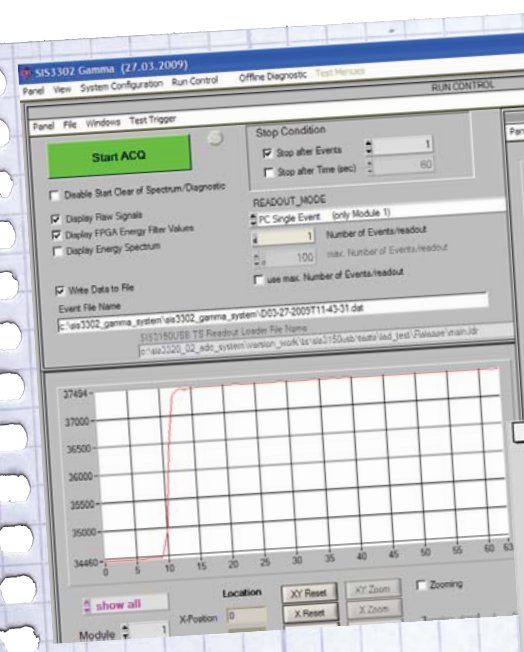
SIS3302 Firmware Implementations

Configuration	Connector Type(s)
Single Ended LEMO	8 x LEMO EPL.00.250.NTN
Single Ended SMA	8 x Telegärtner J01151A0201
Differential 00	8 x LEMO EGG.00.302.CLL
Differential 0S	8 x LEMO EPL.0S.302.HLN
Mixed	4 x EPL.00.250.NTN 4 x LEMO EPL.0S.302.HLN

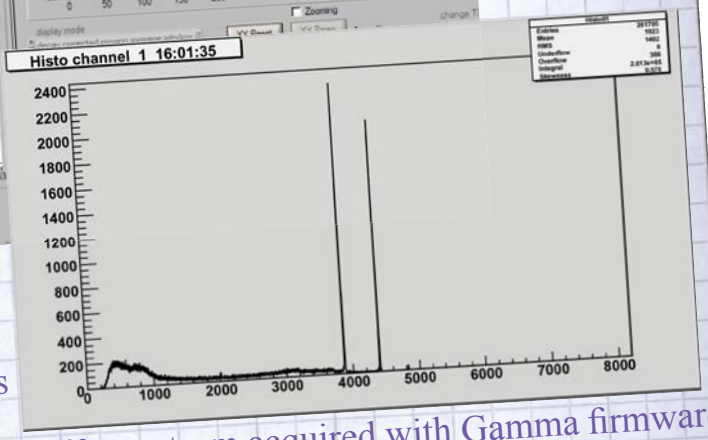
SIS3302 Input Configurations

* Note: Firmware for the SIS3302 with a pulse processing algorithm was developed in a GSI/KVI collaboration and the code is available under www.opencores.org. Feel free to ask about custom development assistance for your application.

SIS3302 User Interface Examples

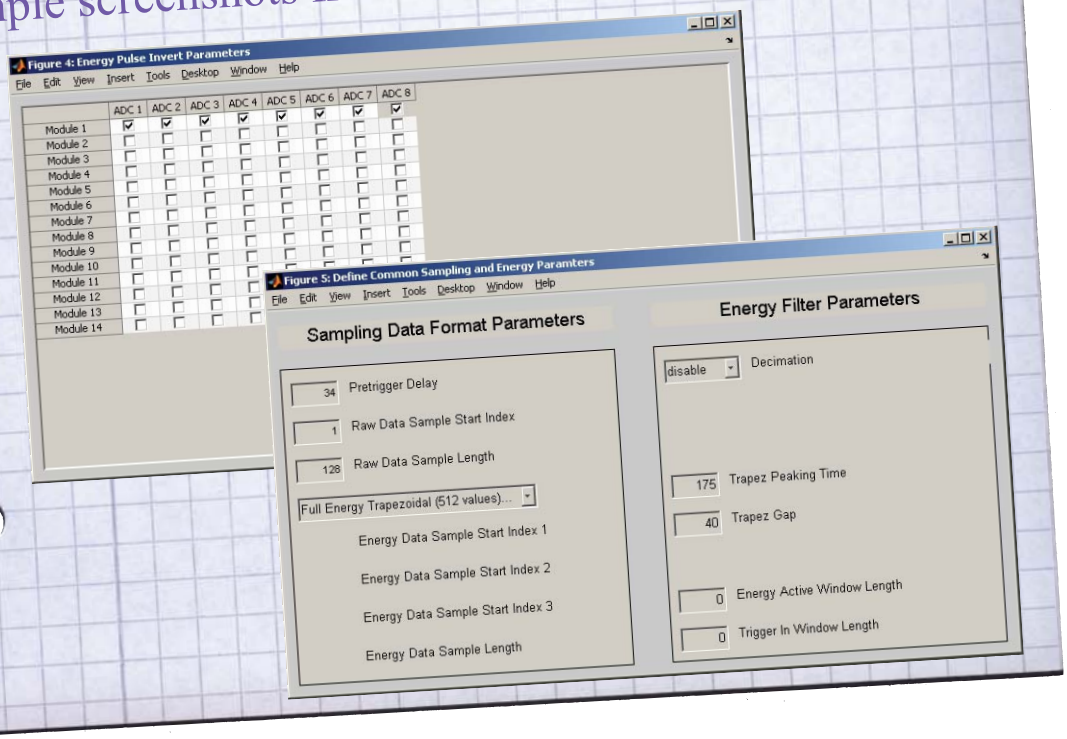


SIS3302 Labwindows CVI Gamma GUI with raw signal and energy filter value screens



Co 60 spectrum acquired with Gamma firmware
(Courtesy of GSI Darmstadt)

Example screenshots from SIS3302 Gamma Matlab GUI

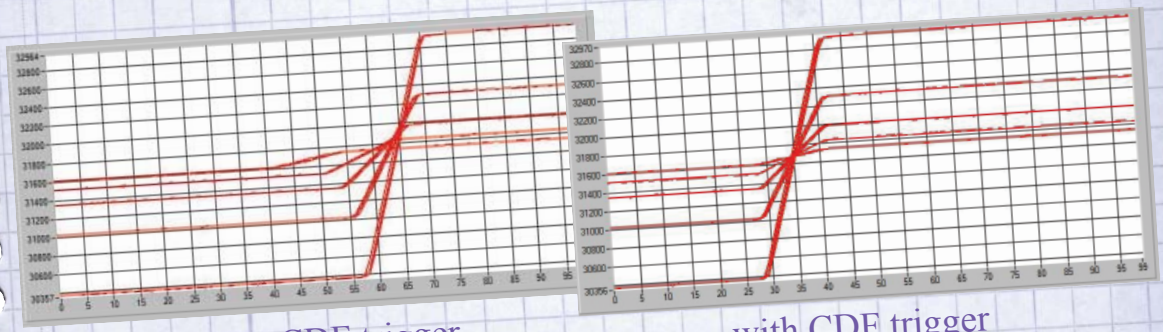


SIS3302 Software/Firmware Examples

Memory bank change with VME broadcast (Gamma firmware)

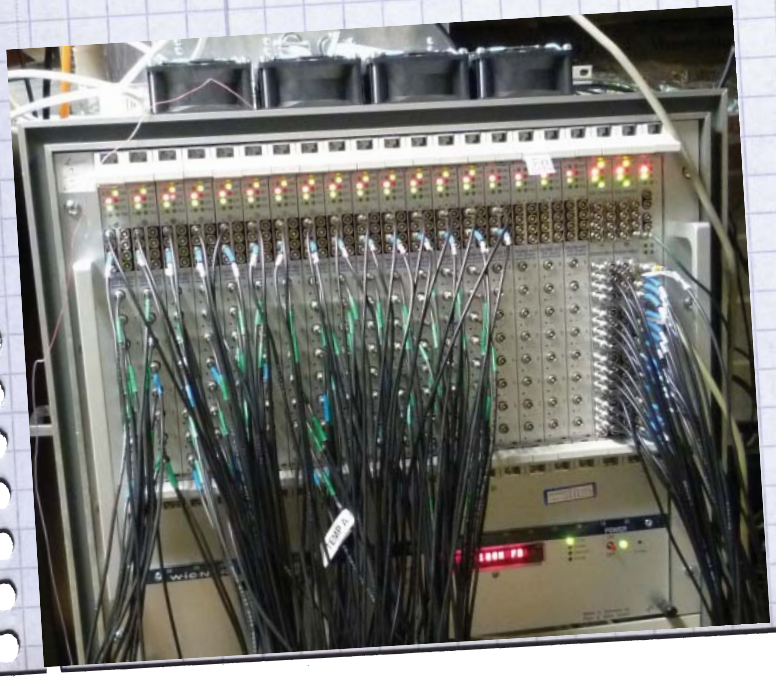
```
if (bank1_armed_flag == 1) {
      addr = gl_uint_SIS3302_BroadcastAddrConf +
                        SIS3302_KEY_DISARM_AND_ARM_BANK2 ;
      bank1_armed_flag = 0; // bank 2 is armed
}
else {
      addr = gl_uint_SIS3302_BroadcastAddrConf +
                        SIS3302_KEY_DISARM_AND_ARM_BANK1 ;
      bank1_armed_flag = 1; // bank 1 is armed
}
if ((error = sub_vme_A32D32_write(addr,0x0 )) != 0) {
      sisVME_ErrorHandling (error, addr, „sub_vme_A32D32_write“) ;
      gl_uint_system_status = SYSTEM_STATUS_MODULES_NOT_READY ;
      return -1 ;
}
```

CFD Trigger (Gamma firmware)



without CDF trigger

with CDF trigger



SIS3302 setup with SIS3820 Clock distributor, SIS3820 trigger distributor and SIS3150 USB to VME interface
(Courtesy University of Wisconsin)

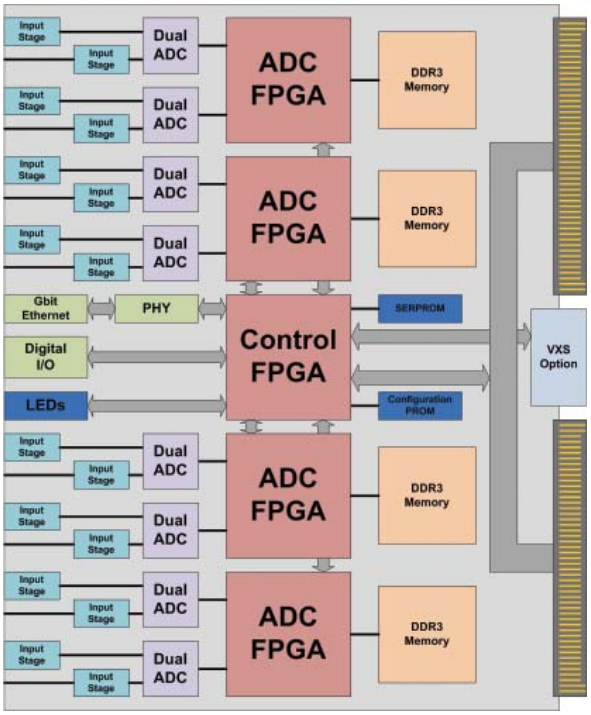
SIS3316 16 Channel VME Digitizer Family
SIS3316-250-14 250 MS/s 14-bit
SIS3316-125-16 125 MS/s 16-bit

With the SIS3316 board family we are doubling the channel density to 16 synchronously sampling digitizer channels per single width VME card. Low power consumption dual ADC chips are used in combination with Xilinx Spartan 6 FPGAs. In addition to a performant VME slave interface a SFP socket allows for high speed point to point readout implementations.

Functionality

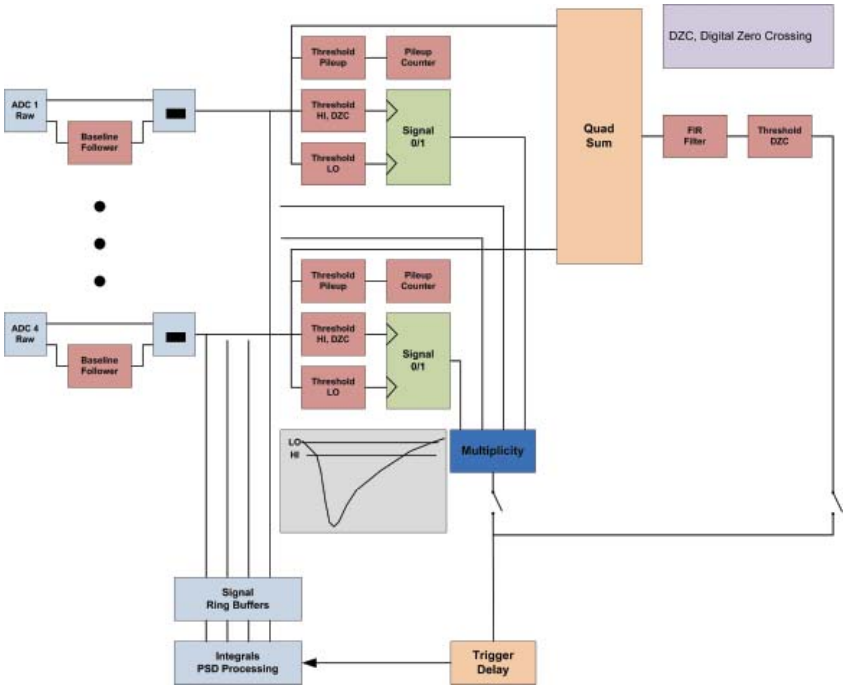
- 16 channels
- 14/16-bit resolution
- 250/125 MSample/s per channel
- > 125/62.5 MHz analog bandwidth
- 32 MSample/channel memory
- programmable offset DACs
- two programmable gain settings
- 50 Ω /high impedance programmable
- internal/external clock
- random clock mode for slow acquisition
- firmware discriminator (16 individual thresholds)
- trigger input and output
- trigger bus
- flexible acquisition and readout modes
- readout in parallel to acquisition
- A32/D32/BLT32/MBLT64/2eSST
- generic and application specific firmware designs
- LEMO 00 connectors (FBM on request)
- SFP socket for high speed link readout
- In field JTAG and VME firmware upgrade

SIS3316



SIS3316 Block Diagram

SIS3316 Firmware Example: Quad Channel PSD



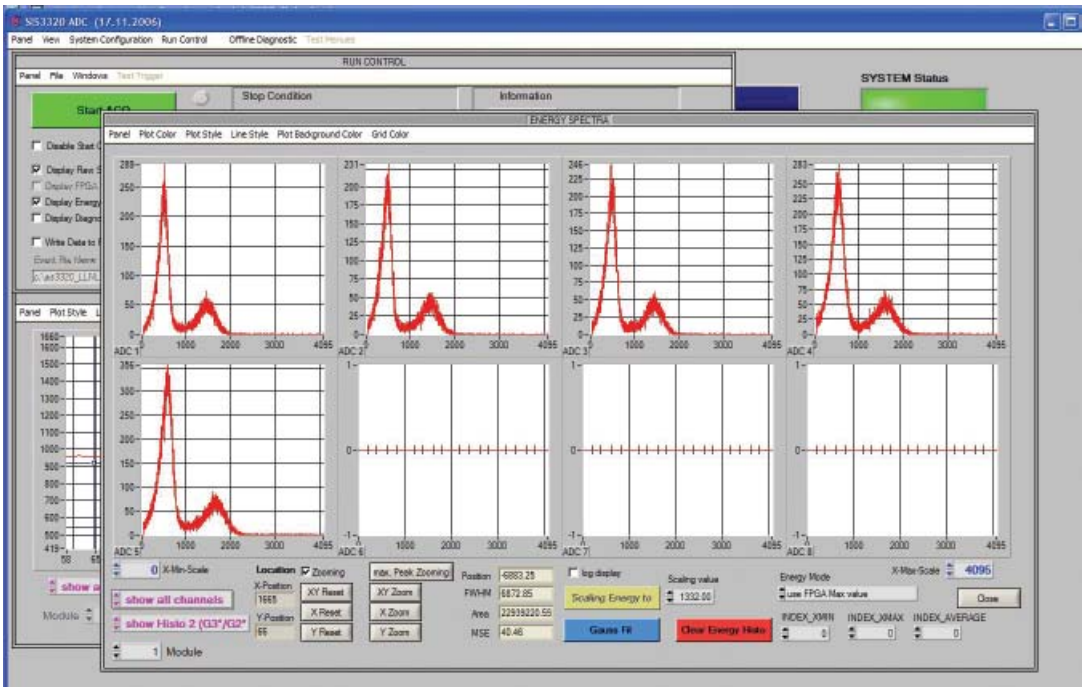
SIS3320-250 8 Channel 250 MS/s 12-bit VME Digitizer

SIS3320-250

The SIS3320-250 is the high speed version of the SIS3302 digitizer. Both cards have the same architecture in common. The SIS3320-250 is typically used in accelerator controls, Neutron/Gamma discrimination setups and other high speed applications.

Functionality

- 8 channels with 12-bit resolution
- 40 - 250 MSample/s per channel
- > 125 MHz analog bandwidth
- 32 MSample/channel memory
- random clock mode for slower acquisition
- programmable offset DACs
- internal/external clock
- trigger input and output
- flexible acquisition and readout features
- readout in parallel to acquisition
- A32/D32/BLT32/MBLT64/2eVME
- generic and application specific firmware designs (see table below)
- LEMO 00 or LEMO 0S connectors (SMA on request)
- firmware discriminator (8 individual thresholds)
- In field JTAG and VME firmware upgrade



SIS3320 Labwindows CVI Neutron/Gamma GUI with signal connected to 5 channels

Major Firmware Id.	Functionality
0x20	8 Channel Generic Digitizer
0x2A	8 Channel Neutron/Gamma
0x31	8 Channel with Accumulators
SIS3320-250 Firmware Implementations	

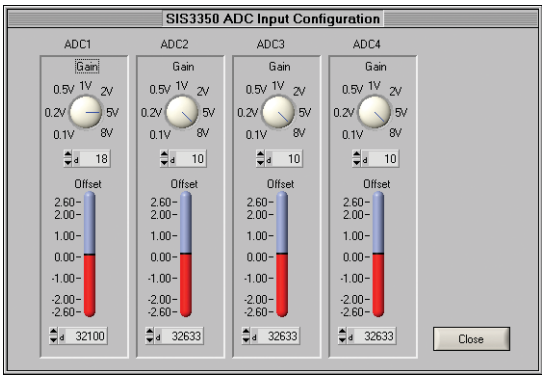
SIS3350 4 Channel 500 MS/s 12-bit VME Digitizer

The SIS3350 is a 4 channel 6U VME digitizer/transient recorder with a sampling rate of up to 500 MS/s per channel and 12-bit resolution. The board has a width of one VME slot. The use of FPGAs for data handling and implementation of the VME interface allows for maximum flexibility. The programmable input stage makes the SIS3350 the card of the choice for flexible lab and test beam setups.

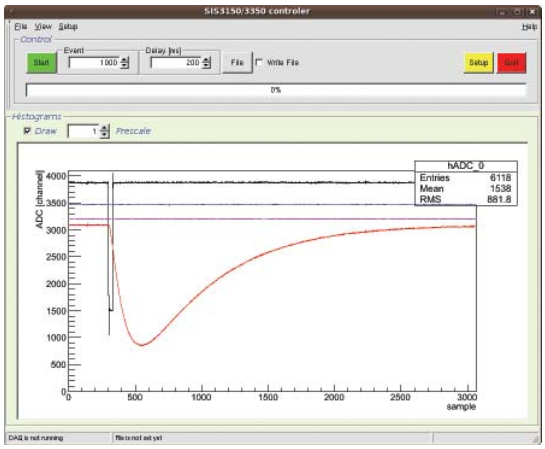
Functionality

- 4 channels
- 12-bit resolution
- 1 to 500 MSample/s per channel
- > 250 MHz analog bandwidth
- internal clock
- external clock with variable threshold
- programmable offset (DACs)
- programmable gain (VGAs)
- 128 MSample/channel memory (512 MSample option)
- multi event mode
- event directory
- autostart capability
- pre/post trigger capability
- 2/4/8/16/32/64/128 sample averaging mode
- trigger generation/output
- additional LVDS in-/outputs
- BNC connectors
- single width 6U VME card
- A32/D32/BLT32/MBLT64/2eVME/SST
- 1/2/4 GBit optical link (SFF LC) option
- 10/100/1000 MBit Ethernet option

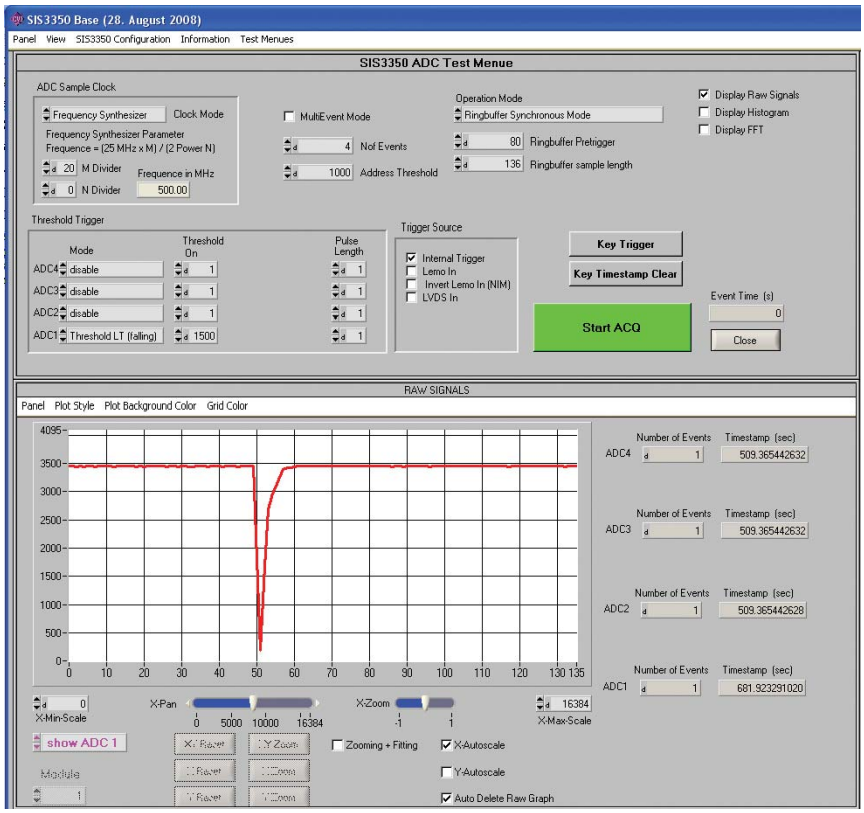
SIS3350



Gain and offset screen of SIS3350 Labwindows CVI GUI



NaI signal in 3150/3350 ROOT control panel (courtesy Dr. Irakli Keshelashvili U. of Basel)



Main screen of SIS3350 base program Labwindows CVI GUI

SIS3305 8 Channel 1.25 GS/s 10-bit VME Digitizer

2/4/8 Channel 5/2.5/1.25 GS/s

The SIS3305 is a dual quad channel ADC chip based digitizer/transient recorder with 10-bit resolution. The four by four cross point switch ADC technology allows for two channel 5 GS/s, four channel 2.5 GS/s and eight channel 1.25 GS/s operation. Xilinx Virtex 5 frontend FPGAs in combination with a Virtex 4 VME interface implementation allow for maximum data handling flexibility.

SIS3305

Functionality

- single width 6U VME card
- 2/4/8 channels
- 5 GS/s, 2.5 GS/s or1.25 GS/s per channel
- 10-bit resolution
- 512/256/128 MSamples/channel memory
- 2 GHz analog bandwidth
- TDC based 27ps fine timing
- 4 channel input stage piggy boards
- SMA connectors for analog inputs
- internal/External clock
- readout in parallel to acquisition
- multi event mode
- individual trigger thresholds
- channel above treshold LEDs
- pre/post trigger capability
- sparsification
- A32/D32/BLT32/MBLT64/2eVME/SST
- in field JTAG and VME firmware upgrade capability

Front Panel Control Signals:

- differential clock output
- differential clock input
- trigger OR output/trigger input
- counter input
- reset counter/time Stamp input
- 1/2/4 GBit/s optical link option
- veto input option

16 Channel 1.25 GS/s SIS3305 System

Miscellaneous

new

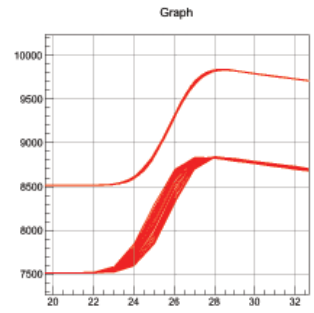
SIS3316-DT 16 Channel Desktop Digitizer

Standalone version based on SIS3316 VME card

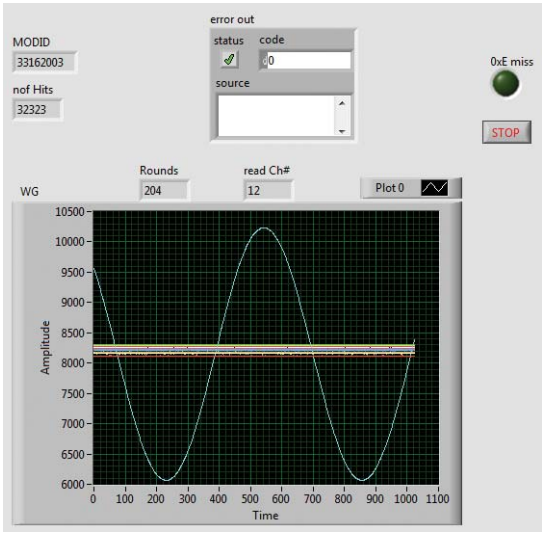
- 19 - 36 V DC Power supply
- 16 channel 250 MSPS 14-bit or
- 16 channel 125 MSPS 16-bit
- GBit/s Ethernet readout (Optical link option)

refer to the SIS3316 VME Digitizer page for other parameters

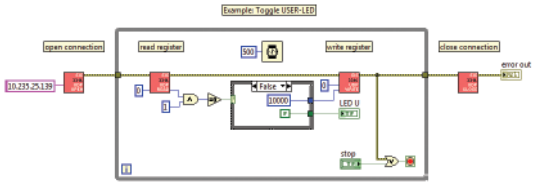
SIS3316-DT



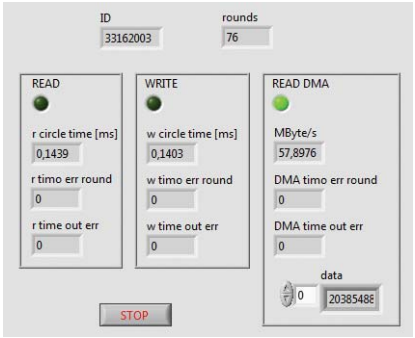
SIS3316 < 70ps FWHM
high resolution
timestamp illustration



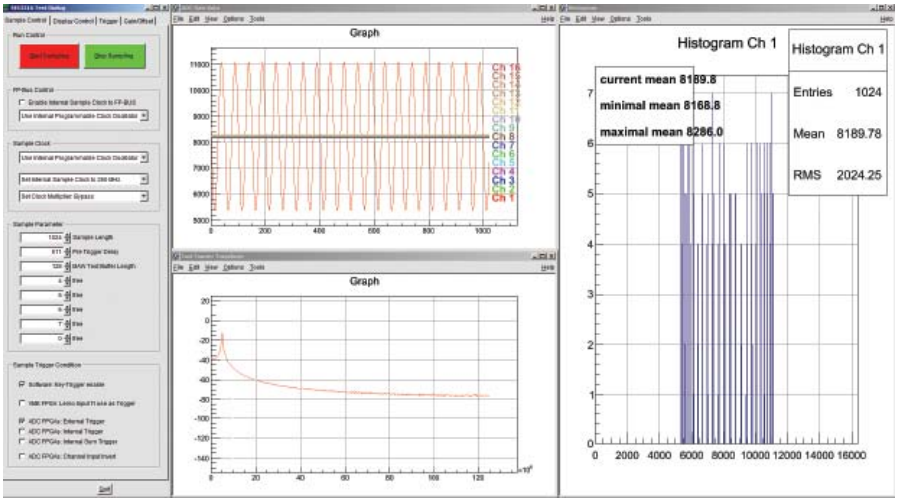
Labview Sampling GUI



Labview VI illustrating register access
(to toggle the user LED)



Labview VI to measure
read/write cycle time and
DMA performance



SIS3316-DT ROOT GUI

FADCRMON Dual 12-bit 250 MS/s Digitizer With Ethernet Connectivity

The FADCRMON digitizer board with Ethernet was originally developed for the DESY PANDORA (Photon And Neutron DOse Rate meter) systems. They are used in radiation protection applications with conventional and pulsed radiation fields like Petra III or FLASH. Complete systems will be available through Berthold Technologies.

FADCRMON

Functionality

- 2 channels of 250 MS/s 12-bit digitizer
- one LEMO TTL input (for scaler applications e.g.)
- 4 TTL inputs
- 2 digital outputs
- Xilinx Virtex 4 based
- Virtex 4 PPC for computing tasks
- 10/100/1000 Ethernet
- 1/2/4 GBit/s SFF link medium option
- DDR2, Flash and EEPROM memory
- diagnostic LEDs
- 2 test push buttons
- application software update over Ethernet
- in field firmware update

Application Examples

- distributed digitizer systems
- standalone digitizer with data processing

Contract Development for DESY
Production under DESY license LV 58

SIS1104 4-Lane PCI Express Quad Optical Link Card

Multiple lane PCI Express cards allow for the implementation of data acquisition hardware with unprecedented performance. The SIS1104 was developed for the readout of data streams from pn-CCD pixel detectors at state of the art X-ray sources like the DESY FLASH. One of the key requirements is loss free high sustained data throughput.

SIS1104

Functionality

- 4-Lane PCI Express
- Xilinx Virtex 5 based
- four 1/2/4 GBit/s SFF link media
- 640 MByte/s sustained throughput with LINUX driver
- 2 GByte buffer memory option

Application examples

- pixel detector readout systems
- frontend data stream receiver
- point to point readout of SIS3305 and SIS3350 digitizer boards

The SIS1104 was developed under contract for the Halbleiterlabor of the Max Planck Gesellschaft

SIS1350 500 MS/s 12-bit PCI Express Digitizer

The SIS1350 is our first PC add on digitizer card. It was developed for high repetition rate acquisition of short analog signals (i.e. up to 128 µs at 500 MSPS) with good resolution.

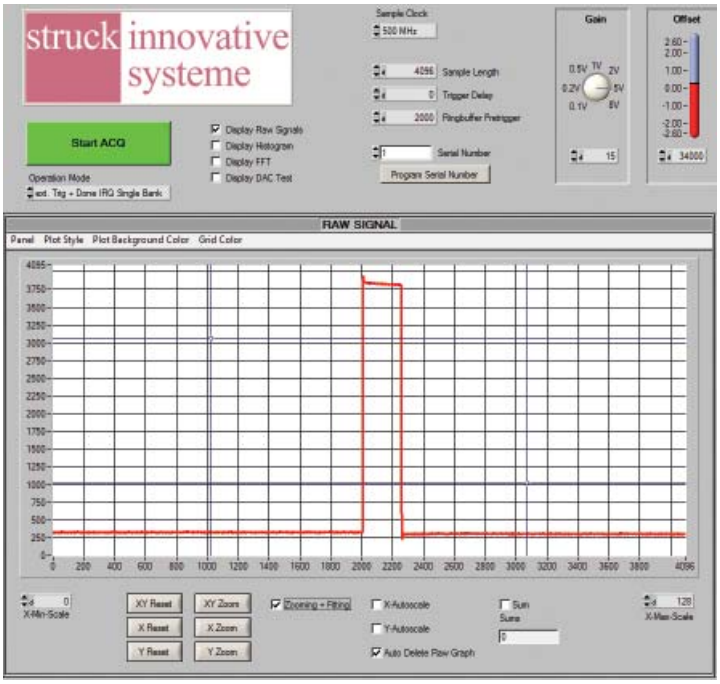
Functionality

- single Lane PCI Express PC add on card implementation
- one channel
- external TTL (SMA connector) and internal trigger
- 500 MS/s (10 MS/s - 500 MS/s)
- 2 x 64 KSamples/channel memory
- offset DAC
- VGA (variable gain amplifier)
- up to 250 MHz analog bandwidth
- ≤ +/- 6 V DC into 50 Ω SMA
- > 9 bit ENOB (@ 9.82Mhz sine FS)
- readout in parallel to acquisition
- dual bank mode
- XILINX Spartan 6 FPGA based
- in field JTAG and PCI EXpress firmware upgrade capability

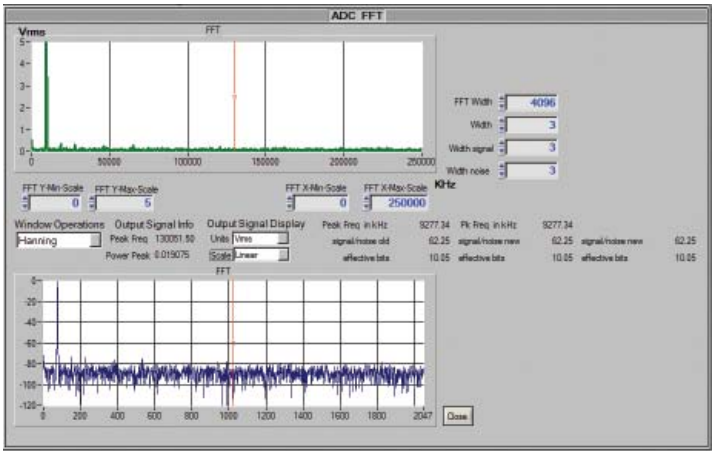
Software Support

- Windows 7 Driver API
- ready to run Labwindows CVI GUI
- more on request

SIS1350 Digitizer



Screenshot of SIS1350 GUI



FFT of 9.28 MHz Sine in SIS1350 GUI

MTCA.4 (µTCA for Physics)
SIS8300 10 channel 16-bit 125 MS/s MTCA.4 Digitizer

ATCA and it's substandards like µTCA play an increasingly important role in the embedded world. The efforts of the PICMG workgroup xTCA for Physics to optimize the standard for next generation accelerators and experiments have resulted in the newly adopted MTCA.4 standard. The SIS8300 digitizer -developed for applications at the European XFEL e.g.- can be regarded as a demonstrator for the new standard.

Functionality

- 4 lane PCI Express connectivity
- 10 channels 125 MS/s 16-bit ADC
- 10 MS/s to 125 MS/s per channel sampling speed
- XC5VLX50T/XC5VSX50T-3FFG1136C Xilinx
- 25 MSample buffer memory per channel
- AC and DC input stage
- ADC inputs through Rear Transition Module (RTM)
- internal, front panel, RTM and backplane clock sources
- two 16-bit DACs for fast feedback implementation
- high precision clock distribution circuitry
- programmable delay of dual channel digitizer groups
- Gigabit link port implementation to backplane
- twin SFP card cage for high speed system interconnects

SIS8300 MTCA.4 Digitizer

Related xTCA Products	Page
SIS8100/3104 µTCA to VME Interface	5
SIS8100 µTCA FMC Carrier	24
SIS8100 µTCA Gigabit Link Card	24
SIS8300-L 125 MSPS 16-bit Digitizer	20
SIS8325 250 MSPS 16-bit Digitizer	20
SIS8900 RTM for SIS8300	22
DWC8300 Downconverter RTM*	23

Name	Source	Description
SIS8900	Struck	Single Ended Input Card
RTM7201	HYTEC	4-channel Signal Modulator
DWC8300	Struck*	Downconverter
BPM	DESY	Interleaved Sampling for BPM readout
APD	DESY	Dual Channel Signal Stretcher
Fast ADC RTM	SLAC	LLRF ADC Frontend

Available RTMs for SIS8300

*under license of DESY

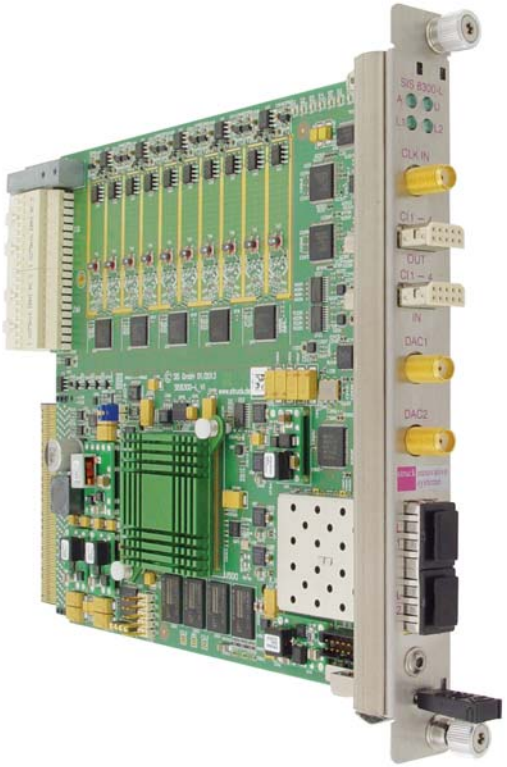
Development in co-operation with DESY
under ZIM Förderkennzeichen 2460101MS9

SIS8300-L 10 channel 16-bit 125 MS/s MTCA.4 Digitizer

The SIS8300-L is a Xilinx Virtex 6 based complement to the SIS8300. It is targeted to applictions with more demanding link speed- and FPGA resource requirements.
Enhancements related to clocking and a change in the memory architecture were implemented while the basic architecture and functionality of the SIS8300 were preserved.

Functionality

- 4 lane PCI Express connectivity
- 10 channels 125 MS/s 16-bit ADC
- 10 MS/s to 125 MS/s per channel sampling speed
- XC6VLX130T-2FFG1156C Xilinx
- 100 MSample DDR3 buffer memory per channel
- AC and DC input stage
- ADC inputs through Rear Transition Module (RTM)
- internal, front panel, RTM and backplane clock sources
- two 16-bit DACs for fast feedback implementation
- Front panel or Zone 3 DAC routing
- FPGA, RTM_CLK4, DIV0 and DIV1 DAC clock sources
- high precision clock distribution circuitry
- programmable delay of dual channel digitizer groups
- Gigabit link port implementation to backplane
- 6.5 GBit/s on point to point links
- extended MGT clocking scheme
- twin SFP card cage for high speed system interconnects
- Front panel grounding block
- Zone 3 class A1.1 compliant



SIS8300-L MTCA.4 Digitizer

Note: A SIS8300-L version without front panel SMA and Harlink connectors is available also.

new

SIS8325 10 channel 16-bit 250 MS/s MTCA.4 Digitizer

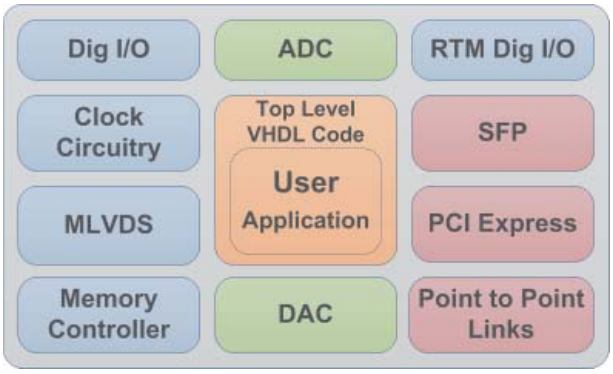
The SIS8325 design doubles the maximum sampling speed of the SIS8300-L. Texas Instruments latest ADS42LB69 digitizer chip is used on the card.
The development is done in a co-operation with DESY in the Helmholtz Validation Funds (HVF) framework.

Functionality

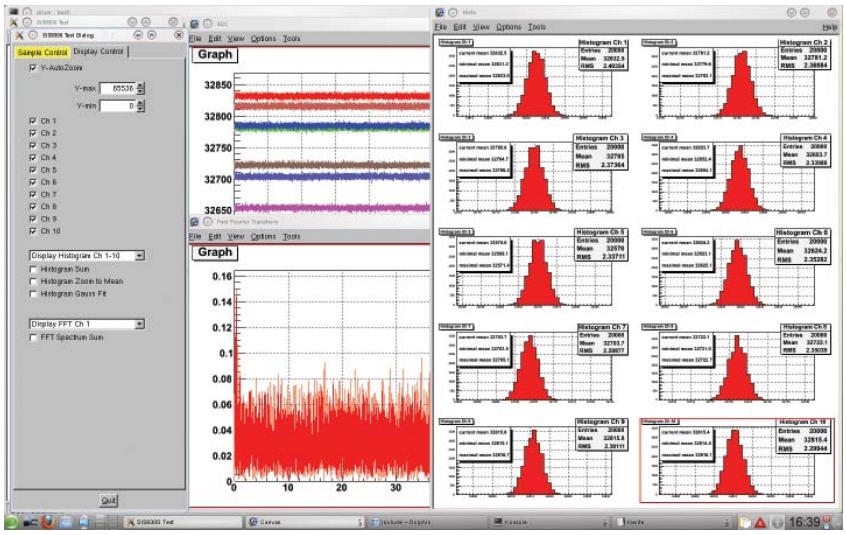
- 4 lane PCI Express connectivity
- 10 channels 250 MS/s 16-bit ADC
- 250 MS/s per channel sampling speed
- XC6VLX130T-2FFG1156C Xilinx
- other parameters like SIS8300-L

SIS8300 Firmware Aspects

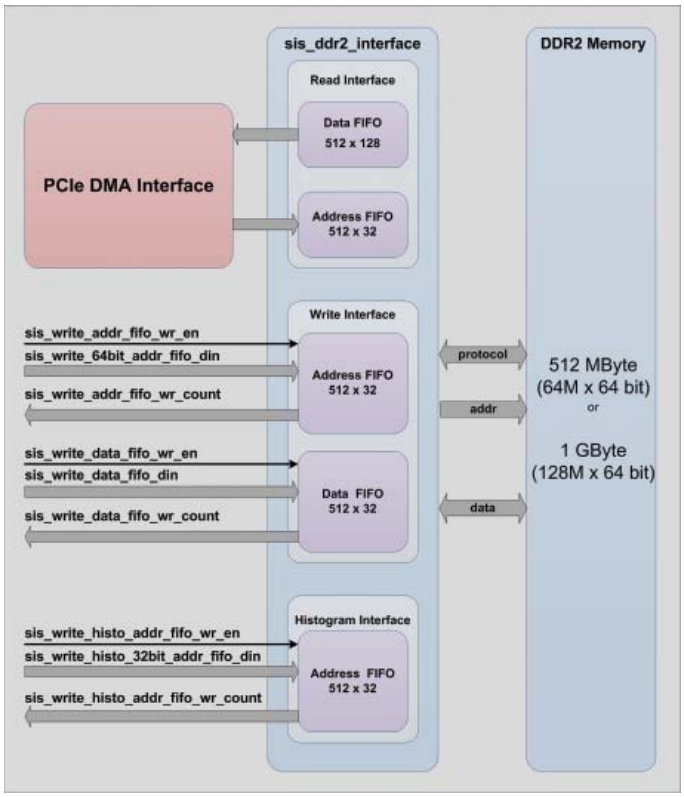
The SIS8300 MTCA.4 digitizer family was developed in co-operation with DESY for a variety of different applications at the European XFEL and demonstrator setups. A modular firmware approach allows for customization targeting the requirements of the specific application. An overview of the firmware building blocks is given in the diagram below.



SIS8300 Firmware Building Blocks



Screen Shot of Generic Firmware SIS8300 ROOT GUI (under LINUX)



SIS8300 Memory Controller Block

DDR2 Memory Controller

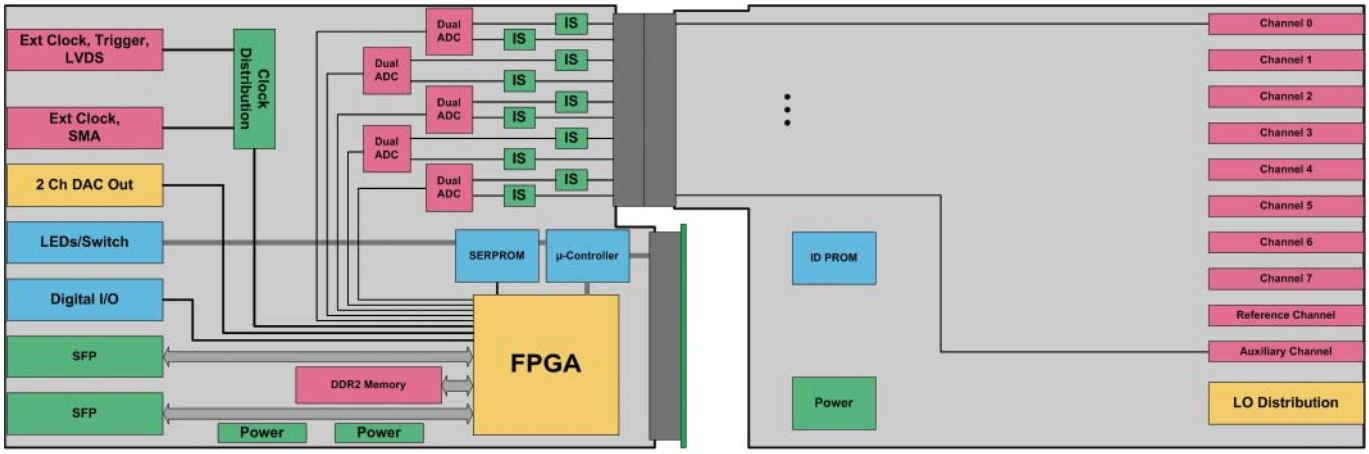
The memory controller block supports the 512 Mbyte and the 1 GByte memory options of the SIS8300. It interfaces to the 4-lane PCI Express with a read/write DMA interface. The histogramming memory controller supports an update rate of 5 MHz (20 MHz within one memory page amid differing three lowest order bits).

Full Custom Firmware

Feel free to inquire about a full custom firmware design development or customized application firmware for the SIS8300 digitizer to meet the requirements for your application.
The UCF file and required information about on board peripherals is provided to those who would like to develop their own full custom firmware design for the card in house.

MTCA.4 Rear Transition Module Concept

The µTCA for Physics Rear Transition Module (RTM) concept is illustrated below. It allows to use the SIS8300 digitizer with a variety of transition boards. Functionality like filtering or down-conversion can be offloaded from an external crate or on board design in a flexible fashion.



SIS8900 MTCA.4 Single Ended Input RTM for SIS8300 Digitizer

The SIS8900 RTM is used to feed single ended -50 Ω terminated- signals to the SIS8300 digitizer. Access to RTM _ CLK0, RTM_CLK1 and RTM_CLK2 and a couple of digital I/O lines is implemented in addition.

Functionality

- MTCA.4 (µTCA for Physics) RTM implementation
- 8-Bit I/O expander for I²C-bus
- 10 LEMO 00 connectors (FBM option)
- 50 Ohm input impedance
- -1 V,...,+1 V default input range
- analog signals can be routed to AC and DC input stage
- RJ45 jack for RTM clocks
- RJ45 jack for Digital I/O
- +5V, 250 mA power option for RJ45 jacks
- two metric on board pin headers for 6 LVDS input/output signals each

SIS8900 RTM

DWC8300 MTCA.4 Downconverter RTM

The DWC8300 is a MTCA.4 downconverter RTM It was developed at DESY for LLRF applications under the designation DRTM-DWC10 and is build by Struck under license of DESY.

Functionality

- MTCA.4 (µTCA for Physics) RTM implementation
- 10 Channels
- 8 Channel FBM multi coax. connector (CH1 to CH8)
- CH0 and CH9 SMA
- 1 GHz - 4 GHz
- Various intermediate frequencies
- Switchable front end attenuators
- LO clock from front panel or RF backplane
- LO power level monitor
- Digitizer clock input (5 - 130 MHz) from front panel or RF backplane
- I2C support
- Class A1.1 compatible

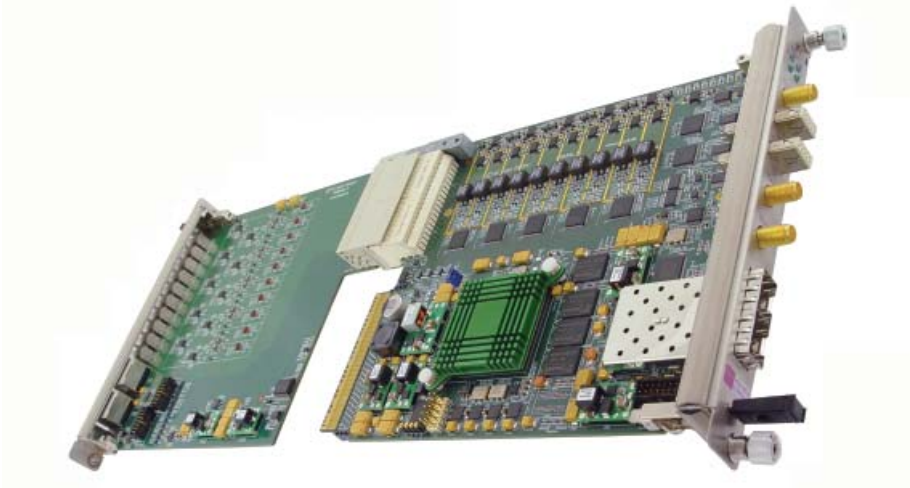
Production under DESY license LV 63

DWC8300 RTM

MTCA.4 / µTCA Systems

We offer turnkey MTCA.4 and µTCA systems with components from different manufacturers as well as system integration and custom designs. The supported operating systems are Windows XP, Windows 7/8 and LINUX.

MTCA.4 (µTCA for Physics) System with CPU, Disk, Digitizers and MCH



SIS8300 MTCA.4 Digtizer with SIS8900 RTM

www.struck.de

µTCA/AdvancedMC

SIS8100 AMC GBit Link Card/VITA 57 FMC Carrier

The SIS8100 is a single width/mid-height AdvancedMC module with single lane PCI Express functionality (AMC.1). The first function is to extend our optical Link family into the xTCA world. The second stuffing option is the single VITA 57 FMC carrier, with target applications like fast I/O.

SIS8100 In Gigabit Link Configuration

Functionality

- AMC.1 AdvancedMC
- single width/mid-height
- PEX8311 PCI Express to local bus bridge chip
- Atmega128 based management
- Xilinx FX20 Virtex 4
- 1/2/4 GBit/s SFF link medium option or
- single FMC carrier option

Applications

- SIS8100/3104 µTCA to VME interface
- frontend data stream receiver
- digital I/O with FMC mezzanine
- analog I/O with FMC mezzanine

Software Support

- Windows XP/7/8
- LINUX
- NI Labview/Labwindows
- VisualC++

follow us at www.twitter.com/struckinnovativ

join our DAQ blog at www.struck.de/blog

subscribe to our RSS feed www.struck.de/struckfeed.xml

Blog

Feed

photographs: struck

Struck Innovative Systeme GmbH
Harksheider Str. 102A
22399 Hamburg
Germany
email: info@struck.de
web: www.struck.de
phone: ++49 40 60 87 305 0
fax: ++49 40 60 87 305 20

rev: 12/13

GL ISO 9001
GL Systems Certification