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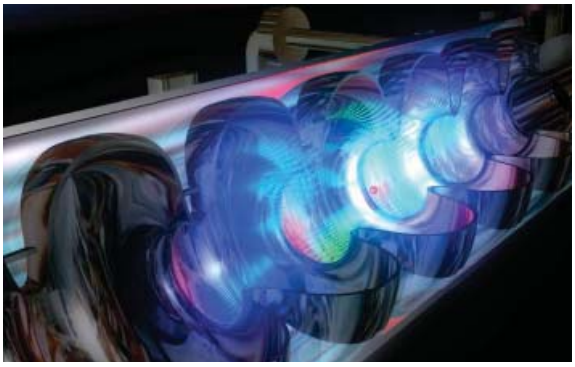
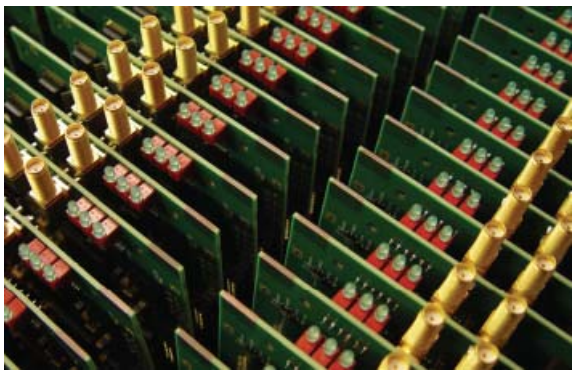
2012: Board Level Electronics Product Highlights



Dear customer and dear probable customer. With this 2012 release the MTCA.4 (µTCA for Physics) is an adopted PICMG standard and we are looking forward to an exciting phase with the deployment of small and large scale MTCA.4 systems. In parallel new VME board developments are going on.

Our Product Range

- VME Interfaces/Bus Couplers/Digital I/O
- VME Digitizers/ADCs
- MTCA.4 Digitizers/ADCs
- USB2.0/3.0 and Ethernet Based Electronics
- PCI Express Cards
- Custom Designs



Application Examples

- Gamma Spectroscopy
- Accelerator Controls
- Synchrotron Radiation
- Neutron Scattering
- Plasma Physics
- Jet Plane Cabin Electronics Testing

Distributors

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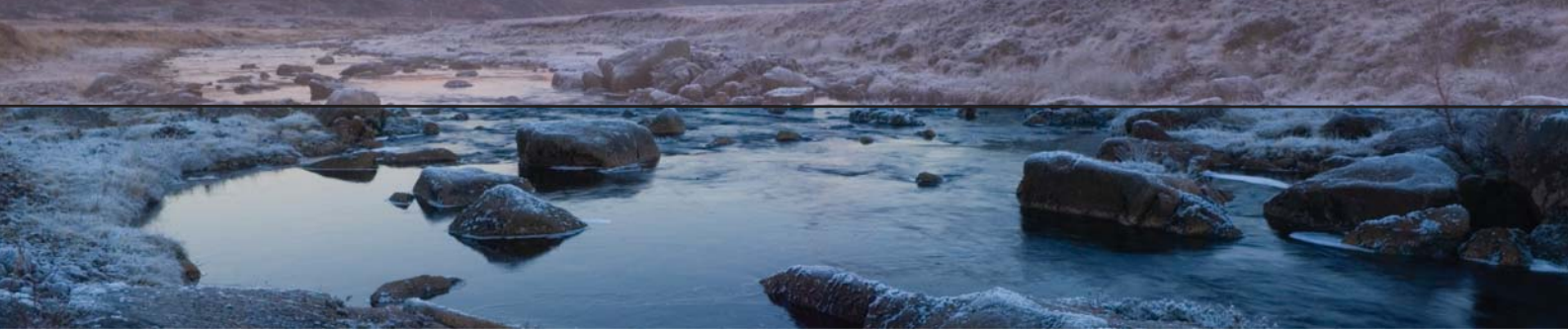


Table of Contents

VME Interfaces/Bus Couplers

SIS3150 USB2.0 to VME Interface

The SIS3150-USB is a high performance USB to VME interface. Connected to a USB2.0 port it supports block transfer speeds in excess of 30 MByte/s. USB1.1 operation is supported also. With the TigerSHARC DSP option it is perfectly suited for hard realtime applications and furnishes 650 ns single cycle access time.

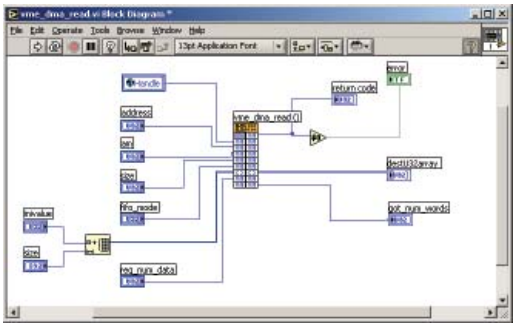
SIS3150USB

Functionality

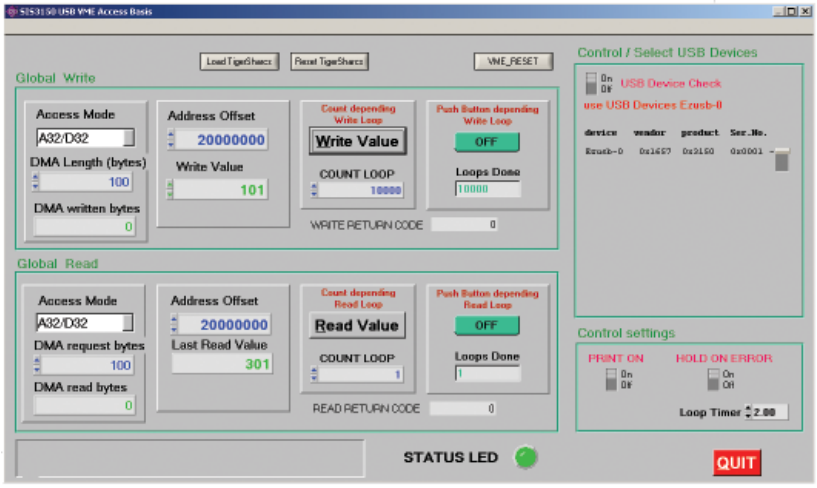
- 2 LEMO control inputs and outputs
- front panel diagnostic LEDs
- one or two TigerSHARC DSP option
- 64 MByte SDRAM w. DSP option
- VME master A16/A24/A32 D8/D16/D32/ BLT32/MBLT64
- VME slave A32 D32/BLT32/MBLT64
- one available CMC site
- P2 access to lower CMC site

Software Support

- Windows XP/Vista/7 and LINUX support
- Labwindows CVI/Labview/Matlab support
- KineticaRT support



Labview Examples: Block Diagram of Block Read



Labwindows CVI Graphical User Interface of SIS3150 base program

new

SIS3153 USB3.0 to VME Interface

The SIS3153 will be the successor to the SIS3150 USB2.0 to VME interface. Backward software compatibility will allow for a smooth migration to the new hardware.

SIS3153

Functionality

- Single width 6U VME master/system controller
- USB3.0/Superspeed USB functionality
- USB2.0 and USB1.1 compatibility
- 2 inputs/2outputs 00 LEMO, NIM/TTL level programmable
- SFP cage for optical or Ethernet link
- (Partial) VME dataway display
- all relevant VME addressing modes up to 2eSST

SIS1100/310x PCI/PCI Express/cPCI/AMC to VME Interface Family

This optical link based PCI/cPCI/PCIe to VME interface card family covers demanding VME data acquisition applications as well as the small laboratory test bench setup. VME readout speeds in excess of 160 MBytes/s are measured in a realistic SST VME master slave setup (SIS3350 ADC as VME slave e.g.). Windows and LINUX drivers in combination with example and user interface code facilitate the migration from other platforms and system integration.

SIS1100e/3104

Common Functionality

- 6U single slot form factor on VME side
- 128 entry mapping table
- VME master A16/A24/A32/D8/D16/D32/BLT32 MBLT64/2eMBLT64/2eSST
- block transfer address auto increment on/off (for FIFO reads)
- system controller function (to be disabled by jumper)
- up to 450 m link distance

Additional SIS3104 features

- SST implementation
- two front panel in- and outputs

Software Support

- Windows XP/Vista/7
- LINUX Kernel 2.6/3.0
- NI Labview/Labwindows
- VisualC++

Interface to	Interface Board	VME Board	Block Transfer Performance
PCI	SIS1100-uCMC/SIS1100-OPT	SIS3100/SIS3104	80 MByte/s
Compact PCI	SIS1100-cCMC/SIS1100-OPT	SIS3100/SIS3104	80 MByte/s
PCI Express	SIS1100-eCMC	SIS3100/SIS3104	80/160 MByte/s
µTCA/AMC	SIS8100	SIS3100/SIS3104	80/160 MByte/s
USB2.0	-	SIS3150USB	30 MByte/s
USB3.0	-	SIS3153	to be determined

VME Interface Overview

The SIS1100/3100 is a co-operative Forschungszentrum Jülich/Struck development.
SIS1100-uCMC and SIS1100-cCMC are produced under FZ-Jülich Lizenzvertrag 27

VME Digital I/O

SIS3820 Multi Purpose Scaler/Digital VME I/O Card

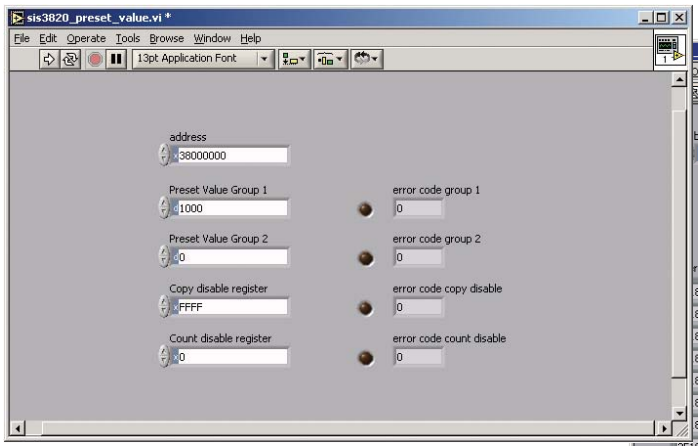
The module is a flexible FPGA based 6U VME board that allows for the implementation of a variety of digital I/O designs. Examples for off the shelf firmware designs are the 32 channel 200 MHz SIS3820-scaler and the 16 channel in/16 channel out SIS3820-latch designs.

SIS3820
LEMO and mixed

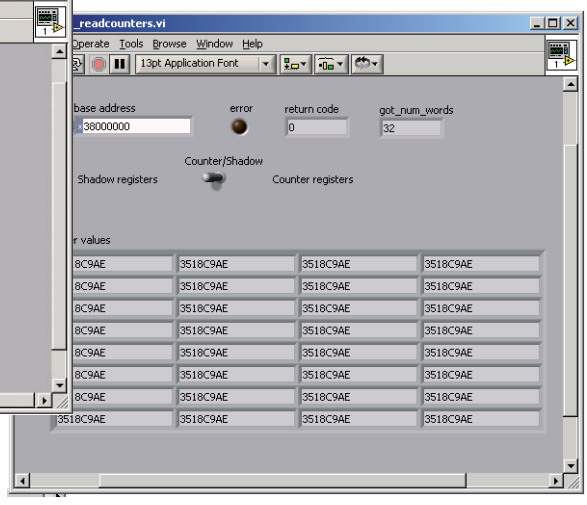
Functionality

- 4 control inputs
- 4 control outputs
- 32 input/output channels + 32 I/Os on P2
- 32 channel 200 MHz scaler/counter implementation
- on board histogramming functionality
- TTL/ECL/NIM/LVDS and other logic level options
- 64/512 MByte SDRAM options
- flat cable, coax. connector and mixed options
- in field firmware upgrade
- A32/D32/BLT32/MBLT64/2eVME
- 80 MBytes/s with SIS1100/3100 in 2e VME
- Windows and LINUX software support for SIS1100/310x interfaces

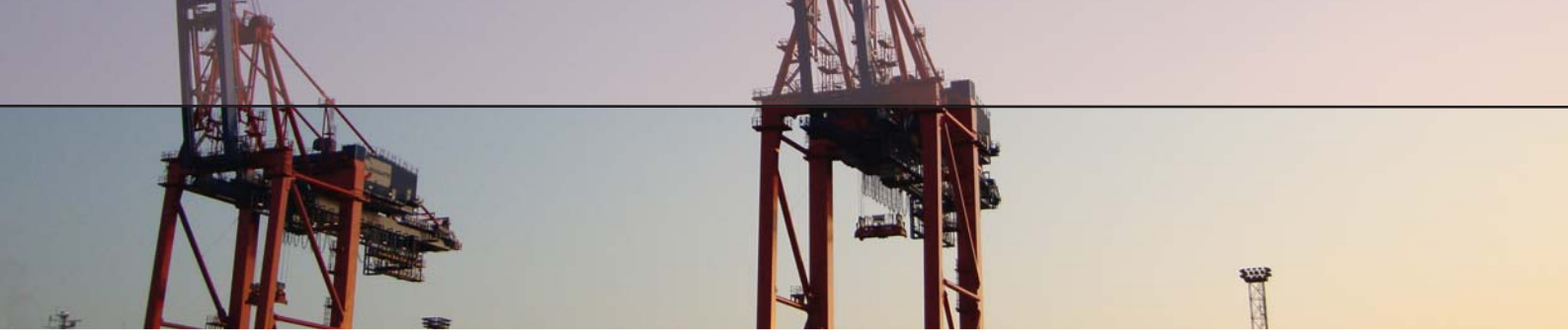
Design	Functionality
SIS3820	32 Channel Multi Purpose Scaler
SIS3820-Clock	Clock Distributor for Digitizers
SIS3820-3600	32-bit Latch w. Counter
SIS3820-3601	16 In/16 Out Register w. 4 Scalers and 4 Flipflops
SIS3820-1500	16 In/48 Out w. Pulse Generators
SIS3820 Firmware Implementations	



SIS3820 Preset Value Labview VI



SIS3820
Read counters
Labview VI
(in 25 MHz test
pulse mode)



SIS3820 Connector Options

Version	Control I/O	Channels 1-16	Channels 1-16
LEMO	LEMO	LEMO	LEMO
Flat Cable	Flat Cable	Flat Cable	Flat Cable
Mixed	LEMO	Flat Cable	Flat Cable
Mixed	LEMO	LEMO	Flat Cable
Mixed	Flat Cable	LEMO	Flat Cable

Table of SIS3820 Connector Options

SIS98xx VME64x Transition Boards

SIS9820 Optical and TTL Output Card

The SIS3820 board has two times 16 I/O lines that are routed from the frontend FPGAs to the P2 connector. They can be accessed by means of VME64x transition cards. An example of a custom design for an accelerator control system is the SIS9820 board.

The SIS9820-V1 (shown to the right) features:
- DC/DC converters to supply +15/-15 V to external hardware
- two 15-pin DSUB connectors with 12 TTL outputs each
- 3 optical outputs with ST connectors

The SIS9820-V2 features:
- additional 4th optical output
- TTL LEMO outputs to monitor optical outputs

SIS9820

SIS9821 32 Channel Input Card

The SIS9821 board feeds 32 signals to the two times 16 I/O lines of the SIS3820 card. In combination with the corresponding firmware it expands the SIS3820 to a 64 channel scaler or 64-bit input register/latch.

The SIS9821 features:
- DC/DC converter to supply negative voltage for NIM/ECL configurations
- power LED
- TTL/ECL/NIM/LVDS and other logic level options
- flat cable, coax. connector and mixed options
- same configuration options as SIS3820 input channels

Feel free to inquire about custom SIS98xx designs

SIS9821

VME Digitizers

VME Digitizer Overview Table

Module	Sampling Speed	Channels	Resolution	Memory
SIS3305	5 GS/s	2	10-bit	512 MSample/channel
SIS3305	2.5 GS/s	4	10-bit	256 MSample/channel
SIS3305	1.25 GS/s	8	10-bit	128 MSample/channel
SIS3350	500 MS/s	4	12-bit	128 MSample/channel
SIS3316-250-14	250 MS/s	16	14-bit	32 MSample/channel
SIS3320-250	250 MS/s	8	12-bit	32 MSample/channel
SIS3316-125-16	125 MS/s	16	16-bit	32 MSample/channel
SIS3302	100 MS/s	8	16-bit	32 MSample/channel
SIS3302-4	100 MS/s	4	16-bit	32 MSample/channel

VME Digitizer Overview

Link to Struck Digitizer Overview Web Page

Typical Common Properties

- Flexible input range configuration
- Single ended and differential inputs on units up to 250 MS/s, single ended on higher sampling speed boards
- Standard analog bandwidth up to Nyquist frequency, reduced or higher bandwidth on request

SIS3300/1 8 Channel 100 MS/s 12/14-bit VME Digitizers

The SIS3300/1 is an 8 channel 6U VME digitizer/transient recorder with a sampling rate of up to 105 MS/s and 12-bit (14-bit respective) resolution. The board has a width of one VME slot. The use of FPGAs for data handling and implementation of the VME interface allows for maximum flexibility.
The SIS3300 and the SIS3301 are legacy cards and it is recommended to use the more recent SIS3302 or the SIS3316 for new digitizer setups.

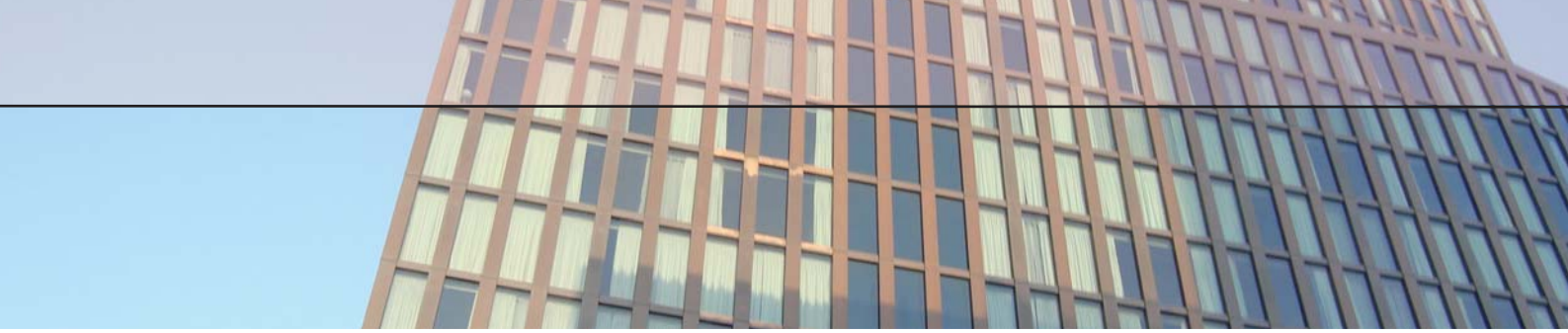
Functionality

- 8 channels with 12-bit/14-bit resolution
- 1 to 105 (15 to 105 respective) MSample/s per channel
- random clock mode for slower acquisition
- > 80 MHz analog bandwidth
- internal/external clock
- 2 x 128 KSamples/channel
- multi event mode
- event directory
- autostart capability
- pre/post trigger capability
- start/stop/gate inputs
- trigger output
- interrupt capability
- A32/D32/BLT32/MBLT64/2eVME
- 80 MByte/s with SIS1100/3100 in 2e VME
- single ended/differential input options
- various input range options
- Windows/LINUX software support for SIS1100/310x interfaces

Custom Firmware Examples

- Medical Imaging
- Amanda Neutrino Detector
- Liquid Argon/Xenon WIMP

SIS3301



SIS3302 8 Channel 100 MS/s 16-bit VME Digitizer

The SIS3302 is our highest resolution digitizer. It embraces high dynamic range measurements as well as high resolution semiconductor spectroscopy and many other applications. A SIS3302 with Gamma firmware harnessing the Multi Channel Analyzer (MCA) implementation is perfectly suited to acquire spectra at synchrotron beamlines in conjunction with a SIS3820 in Multi Channel Scaler (MCS) mode of operation e.g..

SIS3302 and SIS3302-4

Functionality

- 4/8 channels with 16-bit resolution
- 1 - 100 MSamples/s per channel
- random clock mode for slower acquisition
- > 50 MHz analog bandwidth
- 32 MSamples/channel memory
- programmable offset (DACs)
- internal/external clock
- trigger input and output
- refer to the table below for available input configuration options
- flexible acquisition and readout features
- firmware discriminator
- A32/D32/BLT32/MBLT64/2eVME
- generic and application specific firmware designs (see table below)
- custom firmware development support
- in field JTAG and VME firmware* upgrade

Major/Minor Firmware Id.	Functionality
0x01 yy	8 Channel Generic Digitizer
0x14 0y	8 Channel Gamma with MCA
0x14 4y	4 Channel Gamma with MCA
0x15 0y	8 Channel Gamma, long filters
0x31 yy	8 Channel Neutron/Gamma

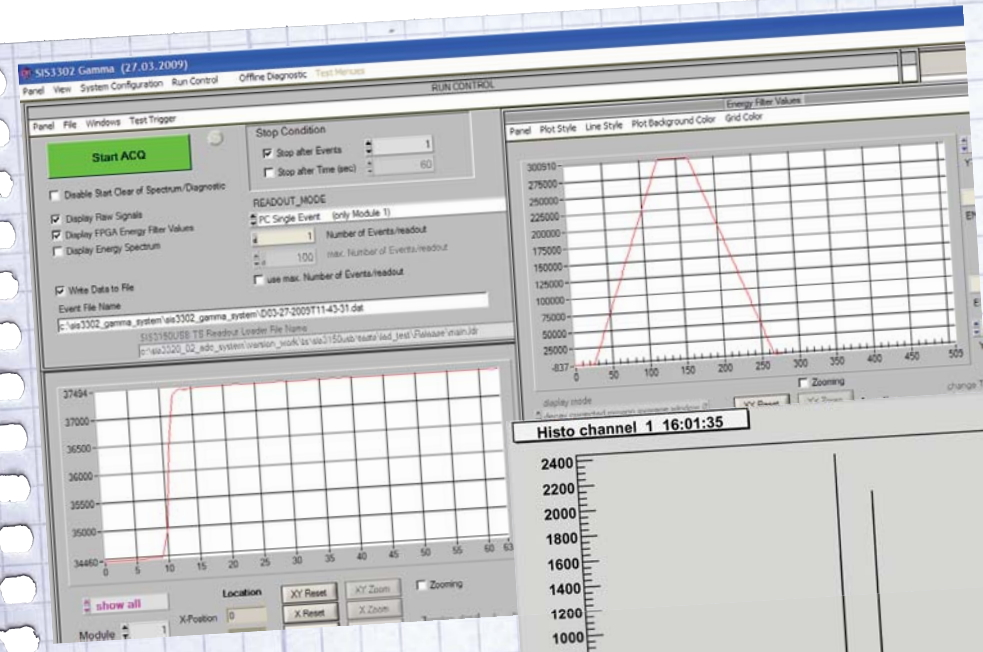
SIS3302 Firmware Implementations

Configuration	Connector Type(s)
Single Ended LEMO	8 x LEMO EPL.00.250.NTN
Single Ended SMA	8 x Telegärtner J01151A0201
Differential 00	8 x LEMO EGG.00.302.CLL
Differential 0S	8 x LEMO EPL.0S.302.HLN
Mixed	4 x EPL.00.250.NTN 4 x LEMO EPL.0S.302.HLN

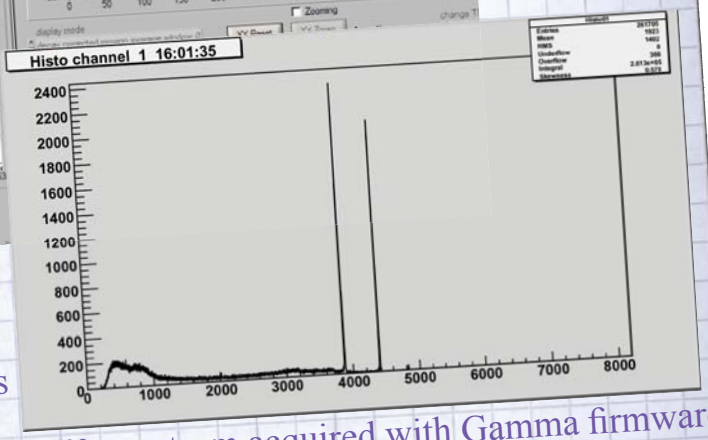
SIS3302 Input Configurations

* Note: Firmware for the SIS3302 with a pulse processing algorithm was developed in a GSI/KVI collaboration and the code is available under www.opencores.org. Feel free to ask about custom development assistance for your application.

SIS3302 User Interface Examples

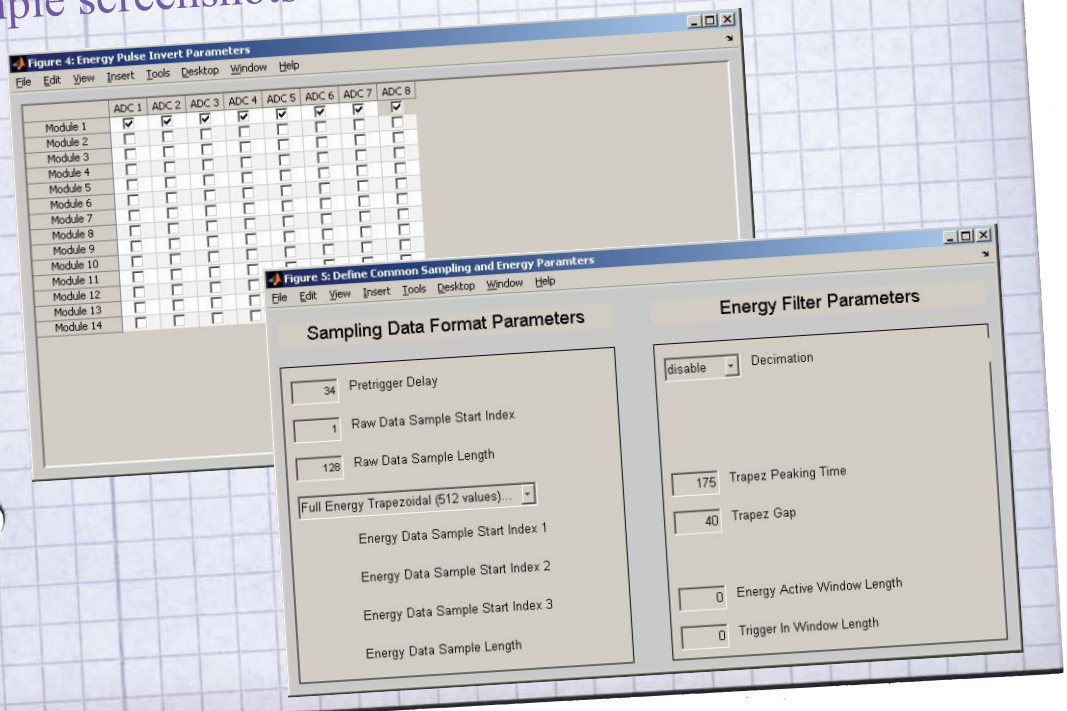


SIS3302 Labwindows CVI Gamma GUI with raw signal and energy filter value screens



Co 60 spectrum acquired with Gamma firmware
(Courtesy of GSI Darmstadt)

Example screenshots from SIS3302 Gamma Matlab GUI

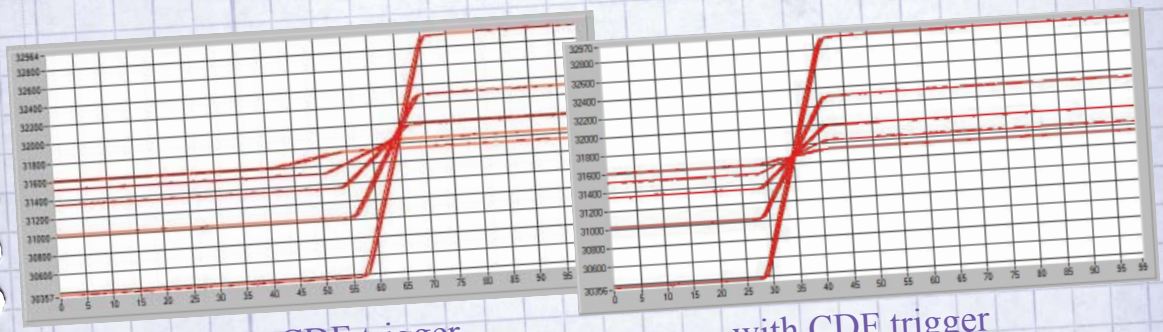


SIS3302 Software/Firmware Examples

Memory bank change with VME broadcast (Gamma firmware)

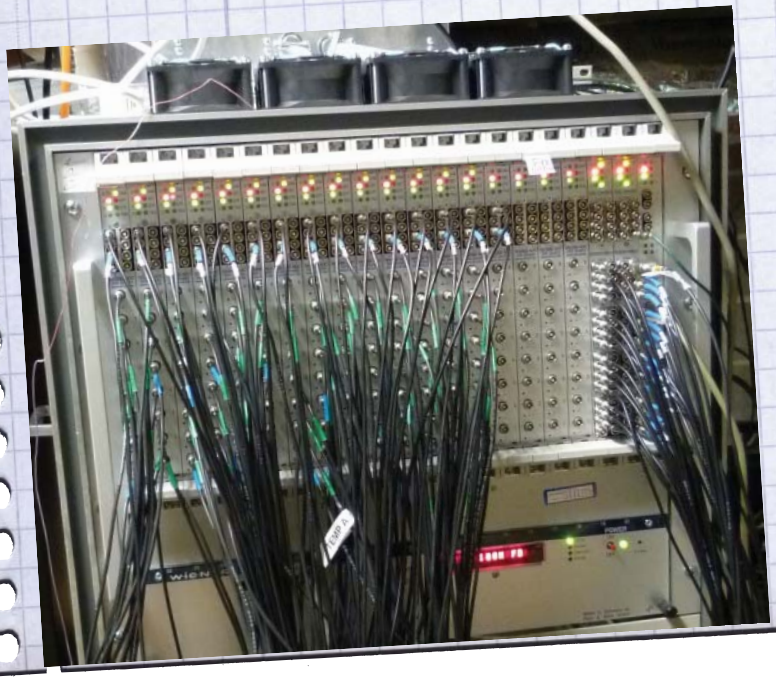
```
if (bank1_armed_flag == 1) {
      addr = gl_uint_SIS3302_BroadcastAddrConf +
                        SIS3302_KEY_DISARM_AND_ARM_BANK2 ;
      bank1_armed_flag = 0; // bank 2 is armed
}
else {
      addr = gl_uint_SIS3302_BroadcastAddrConf +
                        SIS3302_KEY_DISARM_AND_ARM_BANK1 ;
      bank1_armed_flag = 1; // bank 1 is armed
}
if ((error = sub_vme_A32D32_write(addr,0x0 )) != 0) {
      sisVME_ErrorHandling (error, addr, „sub_vme_A32D32_write“) ;
      gl_uint_system_status = SYSTEM_STATUS_MODULES_NOT_READY ;
      return -1 ;
}
```

CFD Trigger (Gamma firmware)

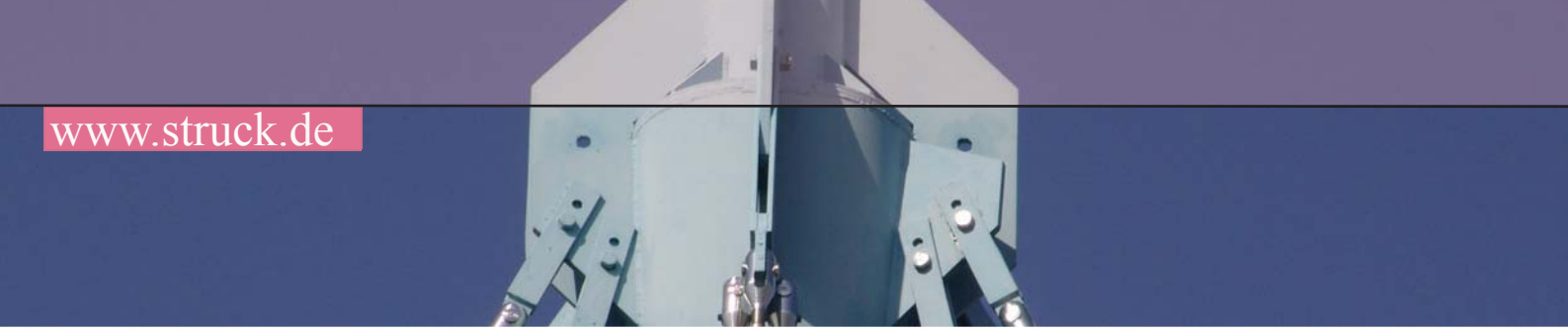


without CDF trigger

with CDF trigger



SIS3302 setup with SIS3820 Clock distributor, SIS3820 trigger distributor and SIS3150 USB to VME interface
(Courtesy University of Wisconsin)



www.struck.de

new

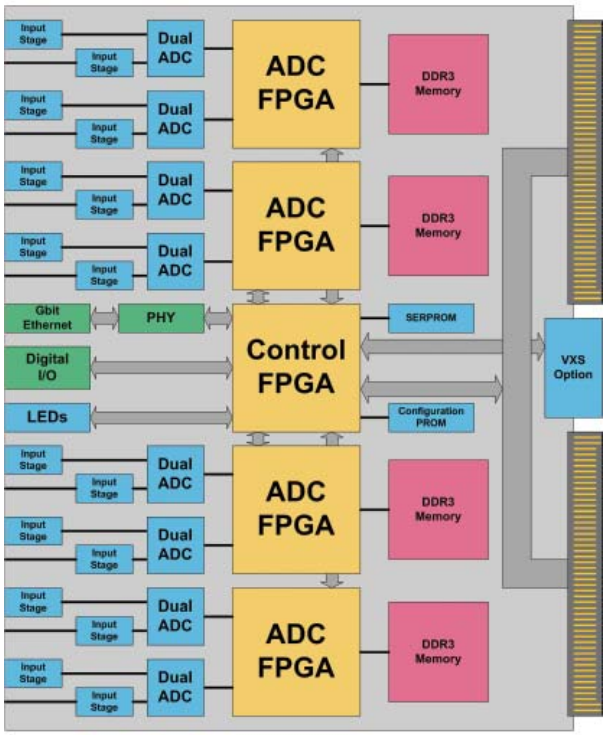
SIS3316 16 Channel VME Digitizer Family
SIS3316-250-14 250 MS/s 14-bit
SIS3316-125-16 125 MS/s 16-bit

With the SIS3316 board family we are doubling the channel density to 16 synchronously sampling digitizer channels per single width VME card. Low power consumption dual ADC chips are used in combination with Xilinx Spartan 6 FPGAs. In addition to a performant VME slave interface a SFP socket allows for high speed point to point readout implementations.

Functionality

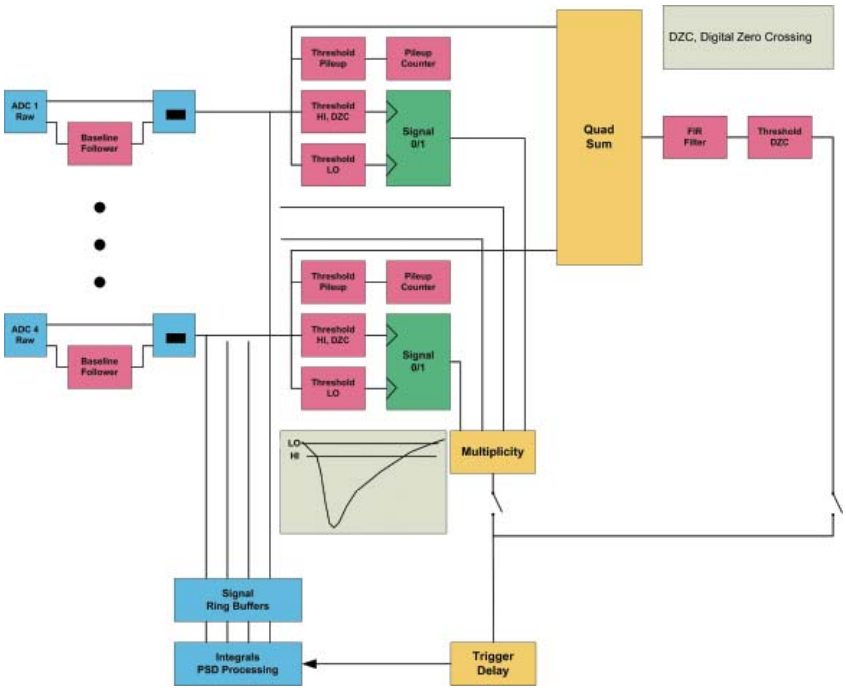
- 16 channels
- 14/16-bit resolution
- 250/125 MSample/s per channel
- > 125/62.5 MHz analog bandwidth
- 32 MSample/channel memory
- programmable offset DACs
- two programmable gain settings
- 50 Ω /high impedance programmable
- internal/external clock
- random clock mode for slow acquisition
- firmware discriminator (16 individual thresholds)
- trigger input and output
- trigger bus
- flexible acquisition and readout modes
- readout in parallel to acquisition
- A32/D32/BLT32/MBLT64/2eSST
- generic and application specific firmware designs
- LEMO 00 connectors (FBM on request)
- SFP socket for high speed link readout
- In field JTAG and VME firmware upgrade

SIS3316



SIS3316 Block Diagram

SIS3316 Firmware Example: Quad Channel PSD



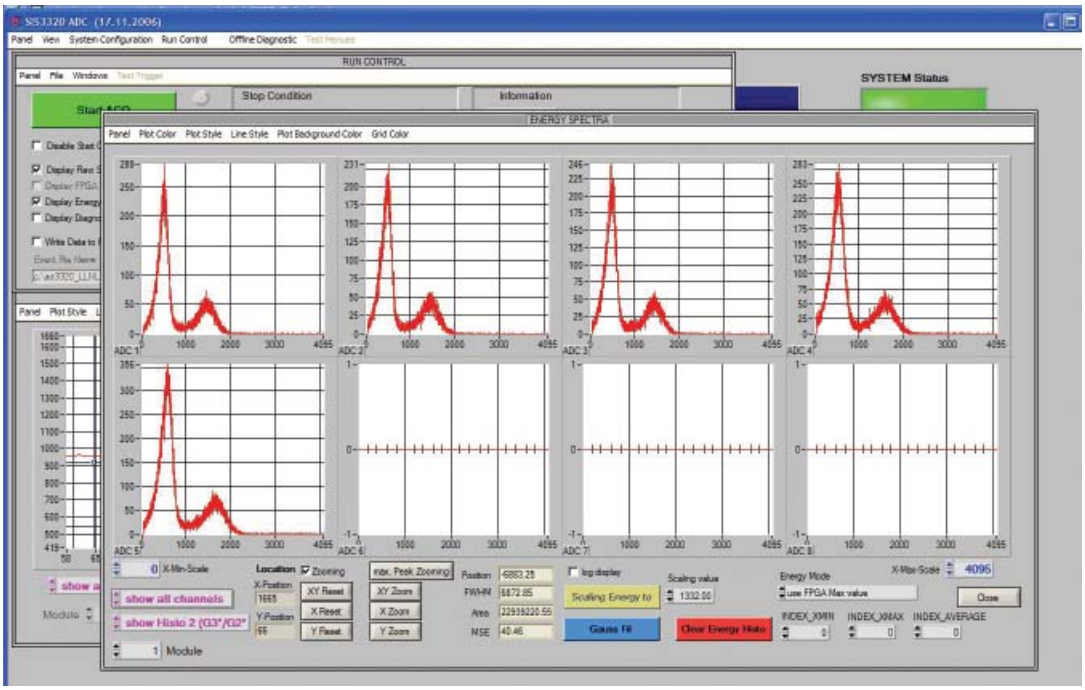
SIS3320-250 8 Channel 250 MS/s 12-bit VME Digitizer

SIS3320-250

The SIS3320-250 is the high speed version of the SIS3302 digitizer. Both cards have the same architecture in common. The SIS3320-250 is typically used in accelerator controls, Neutron/Gamma discrimination setups and other high speed applications.

Functionality

- 8 channels with 12-bit resolution
- 40 - 250 MSample/s per channel
- > 125 MHz analog bandwidth
- 32 MSample/channel memory
- random clock mode for slower acquisition
- programmable offset DACs
- internal/external clock
- trigger input and output
- flexible acquisition and readout features
- readout in parallel to acquisition
- A32/D32/BLT32/MBLT64/2eVME
- generic and application specific firmware designs (see table below)
- LEMO 00 or LEMO 0S connectors (SMA on request)
- firmware discriminator (8 individual thresholds)
- In field JTAG and VME firmware upgrade



SIS3320 Labwindows CVI Neutron/Gamma GUI with signal connected to 5 channels

Major Firmware Id.	Functionality
0x20	8 Channel Generic Digitizer
0x2A	8 Channel Neutron/Gamma
0x31	8 Channel with Accumulators
SIS3320-250 Firmware Implementations	

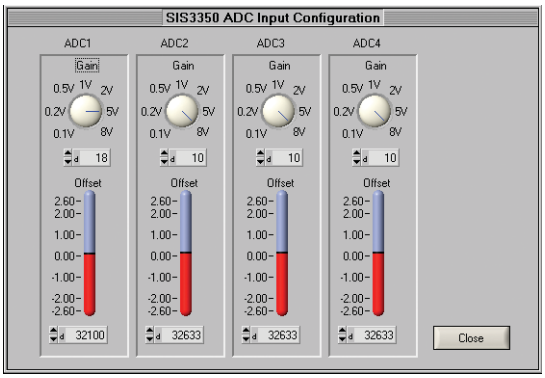
SIS3350 4 Channel 500 MS/s 12-bit VME Digitizer

The SIS3350 is a 4 channel 6U VME digitizer/transient recorder with a sampling rate of up to 500 MS/s per channel and 12-bit resolution. The board has a width of one VME slot. The use of FPGAs for data handling and implementation of the VME interface allows for maximum flexibility. The programmable input stage makes the SIS3350 the card of the choice for flexible lab and test beam setups.

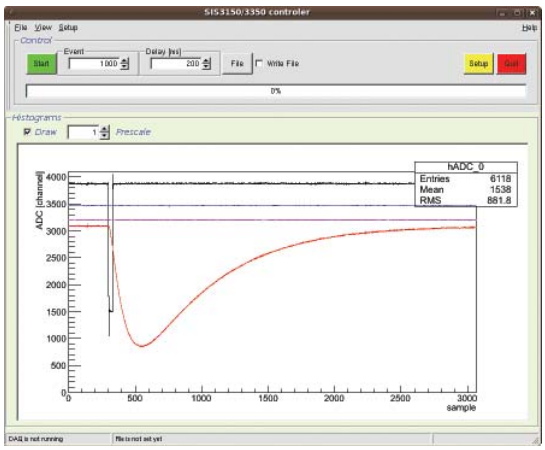
Functionality

- 4 channels
- 12-bit resolution
- 1 to 500 MSample/s per channel
- > 250 MHz analog bandwidth
- internal clock
- external clock with variable threshold
- programmable offset (DACs)
- programmable gain (VGAs)
- 128 MSample/channel memory (512 MSample option)
- multi event mode
- event directory
- autostart capability
- pre/post trigger capability
- 2/4/8/16/32/64/128 sample averaging mode
- trigger generation/output
- additional LVDS in-/outputs
- BNC connectors
- single width 6U VME card
- A32/D32/BLT32/MBLT64/2eVME/SST
- 1/2/4 GBit optical link (SFF LC) option
- 10/100/1000 MBit Ethernet option

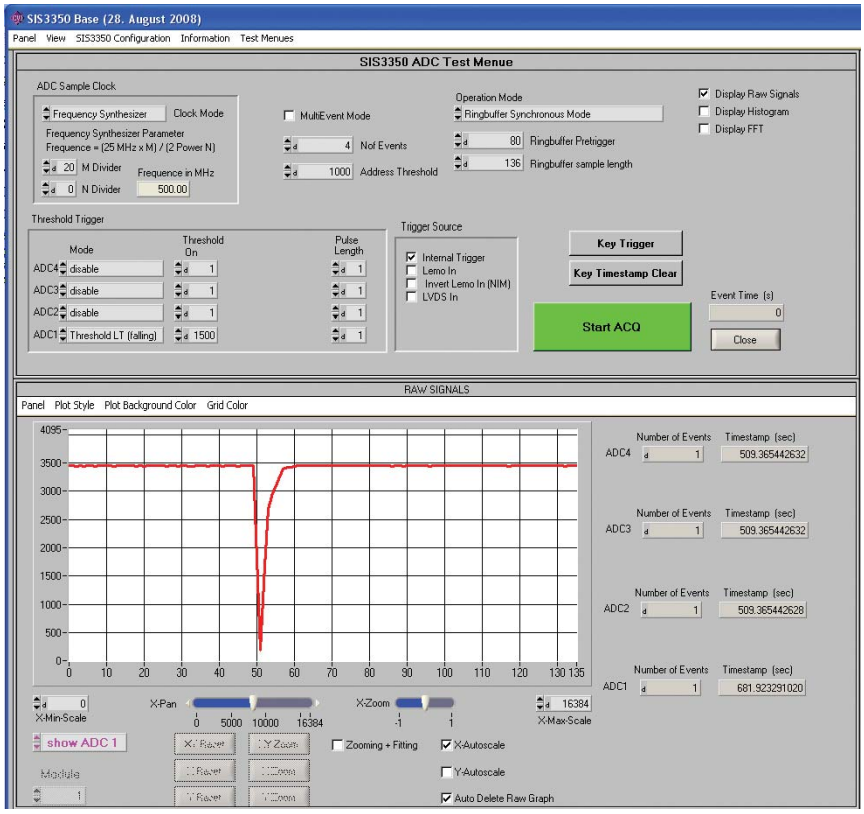
SIS3350



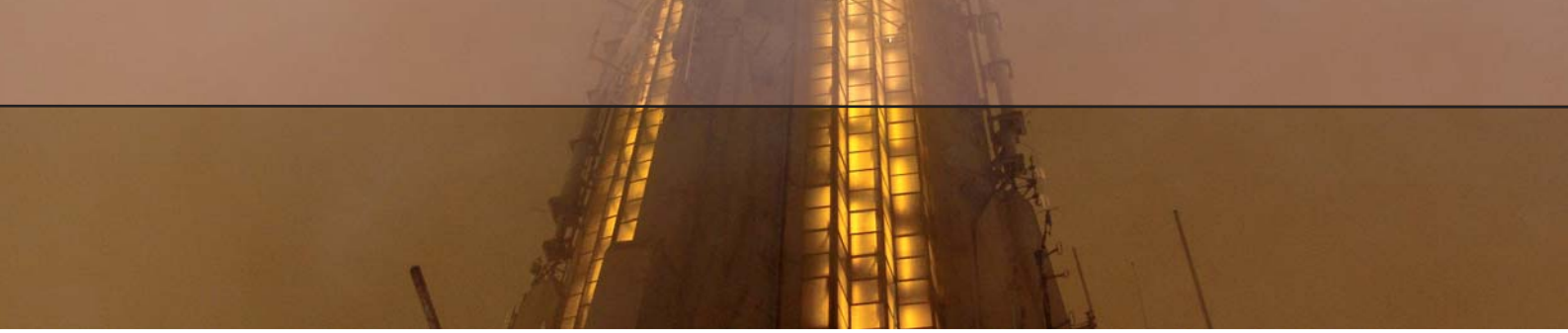
Gain and offset screen of SIS3350 Labwindows CVI GUI



NaI signal in 3150/3350 ROOT control panel (courtesy Dr. Irakli Keshelashvili U. of Basel)



Main screen of SIS3350 base program Labwindows CVI GUI



SIS3305 8 Channel 1.25 GS/s 10-bit VME Digitizer

2/4/8 Channel 5/2.5/1.25 GS/s

The SIS3305 is a dual quad channel ADC chip based digitizer/transient recorder with 10-bit resolution. The four by four cross point switch ADC technology allows for two channel 5 GS/s, four channel 2.5 GS/s and eight channel 1.25 GS/s operation. Xilinx Virtex 5 frontend FPGAs in combination with a Virtex 4 VME interface implementation allow for maximum data handling flexibility.

SIS3305

Functionality

- single width 6U VME card
- 2/4/8 channels
- 5 GS/s, 2.5 GS/s or1.25 GS/s per channel
- 10-bit resolution
- 512/256/128 MSamples/channel memory
- 2 GHz analog bandwidth
- 4 channel input stage piggy boards
- SMA connectors for analog inputs
- internal/External clock
- readout in parallel to acquisition
- multi event mode
- individual trigger thresholds
- channel above treshold LEDs
- pre/post trigger capability
- sparsification
- A32/D32/BLT32/MBLT64/2eVME/SST
- in field JTAG and VME firmware upgrade capability

Front Panel Control Signals:

- differential clock output
- differential clock input
- trigger OR output/trigger input
- counter input
- reset counter/time Stamp input
- 1/2/4 GBit/s optical link option
- veto input option

16 Channel 1.25 GS/s SIS3305 System

Miscellaneous

SIS3150 Dual TigerSHARC Twin CMC Carrier

The SIS3150 is a versatile building block for VME based data acquisition systems. It combines substantial DSP computing power with a high speed VME master/slave implementation and the modular mezzanine (CMC, IEEE 1386) concept.

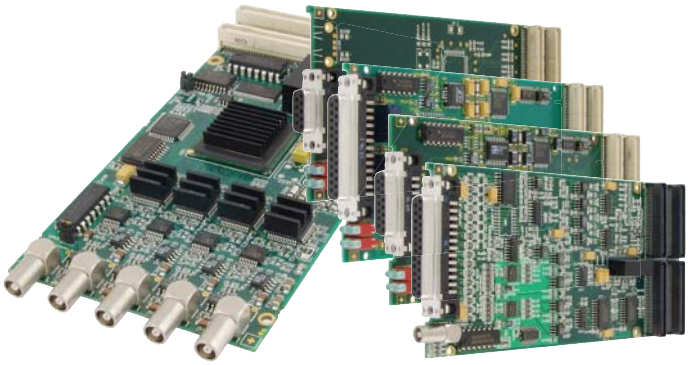
Functionality

- VME A32 D32/BLT32/MBLT64/2eVME (others on request)
- 2 CMC sites
- up to 2 TigerSHARC signal processors (clocked at 250 MHz)
- 64 MBytes SDRAM (requires TigerSHARC memory controller)
- FLASH memory
- front panel I/O option
  2 LEMO inputs and 2 LEMO outputs
- P2 I/O option
  16 single ended or 8 differential inputs per CMC
  16 single ended or 8 differential outputs per CMC
- interrupt capability
- hot swap (in VME64 environments)

SIS3150 with 2 DSPs

SIS9300/992x/9930 CMC Mezzanines for SIS3150

The CMC mezzanine approach in combination with direct access to FPGA or DSP resources -i.e. without involved PCI or PCI Express bridges- allows for the implementation of high performance frontend interface cards with moderate glue logic design effort. A range of Struck CMCs was developed over the last couple of years in the context of different projects.
This successful approach was adopted by the VITA 57 FMC (FPGA Mezzanine Card) standard more recently.
Related product: SIS8100 FMC carrier, see page 16.



SIS9300 and 992x/9930 CMCs

Module	Functionality	Application Example
SIS9300	4 Channel 100 MS/s 14-bit Digitizer	Germanium Detector Readout
SIS9920	Ethernet Interface	Jet Plane Cabin Electronics Testing
SIS9921-RS485	RS485 Interface	Optical Sensor Head Readout
SIS9921-USB	USB Interface	SIS3150USB Interface
SIS9922	RS485 Interface With Relais	Jet Plane Cabin Electronics Testing
SIS9930	Digital I/O	RSIS Grinder Inspection System

Available CMC Mezzanines

Feel free to inquire about a custom CMC development for your application

SIS9965 USB2.0 Based Digital I/O Card With FPGA

The SIS9965 is a single Euro form factor FPGA board with USB2.0 communication interface.

Functionality

- C-rail/standalone mount
- USB2.0
- 8 channels of 24V digital inputs (opto-decoupled)
- 8 channels of 24V digital outputs (opto-decoupled)
- 4 channels of TTL inputs (high impedance)
- 4 channels of TTL Outputs (standard TTL)
- 4 channels of TTL 50 Ohm inputs
- 4 channels of TTL 50 Ohm outputs
- 4 channels of RS422 inputs A+/A-, B+/B-, Z+/Z-, Reserve+/- (opto-decoupled)
- one channel RS422 output (e.g. Clock Out) (opto-decoupled)
- Xilinx FPGA
- +5V supply, +24V depending on external ciruitry
- in field JTAG firmware upgrade capability

SIS9965
mounted in DIN rail fixture

Application Example:
Shaft encoder clock multiplier/divider in aluminum rolling mill instrumentation

SIS9967 USB2.0 16-channel 50 MS/s 14-bit Digitizer

The SIS9967 is a standalone 16 channel 14-bit digitizer card with USB2.0 and optical link readout capabilities. Two 125 MS/s 12-bit DAC channels allow for control of external hardware and/or implementation of fast feedback systems. The card can be used in a desktop enclosure with a 15-19.5V laptop power supply or integrated into a wall mount installation.

Functionality

- double Euro form factor
- 16 channels
- 50 MS/s per channel
- 14-bit resolution
- USB2.0 or optical link connection
- 2 channels 125 MS/s 12-bit DAC
- internal/external clock
- clock output
- 8-bit digital input
- 5-bit digital output
- 8 RS422/485 serial I/Os
- servo motor control
- 15-19.5 V supply voltage
- Xilinx Virtex IV FPGA
- in field JTAG and VME firmware upgrade capability

SIS9967 with
Optical Link
Medium

Application Laser Scanner

FADCRMON Dual 12-bit 250 MS/s Digitizer With Ethernet Connectivity

The FADCRMON digitizer board with Ethernet was originally developed for the DESY PANDORA (Photon And Neutron DOse Rate meter) systems. They are used in radiation protection applications with conventional and pulsed radiation fields like Petra III or FLASH. Complete systems will be available through Berthold Technologies.

FADCRMON

Functionality

- 2 channels of 250 MS/s 12-bit digitizer
- one LEMO TTL input (for scaler applications e.g.)
- 4 TTL inputs
- 2 digital outputs
- Xilinx Virtex 4 based
- Virtex 4 PPC for computing tasks
- 10/100/1000 Ethernet
- 1/2/4 GBit/s SFF link medium option
- DDR2, Flash and EEPROM memory
- diagnostic LEDs
- 2 test push buttons
- application software update over Ethernet
- in field firmware update

Application Examples

- distributed digitizer systems
- standalone digitizer with data processing

Contract Development for DESY
Production under DESY license LV 58

SIS1104 4-Lane PCI Express Quad Optical Link Card

Multiple lane PCI Express cards allow for the implementation of data acquisition hardware with unprecedented performance. The SIS1104 was developed for the readout of data streams from pn-CCD pixel detectors at state of the art X-ray sources like the DESY FLASH. One of the key requirements is loss free high sustained data throughput.

SIS1104

Functionality

- 4-Lane PCI Express
- Xilinx Virtex 5 based
- four 1/2/4 GBit/s SFF link media
- 640 MByte/s sustained throughput with LINUX driver
- 2 GByte buffer memory option

Application examples

- pixel detector readout systems
- frontend data stream receiver
- point to point readout of SIS3305 and SIS3350 digitizer boards

The SIS1104 was developed under contract for the Halbleiterlabor of the Max Planck Gesellschaft

new

SIS1350 500 MS/s 12-bit PCI Express Digitizer

The SIS1350 is our first PC add on digitizer card. It was developed for high repetition rate acquisition of short analog signals (i.e. up to 128 µs at 500 MSPS) with good resolution.

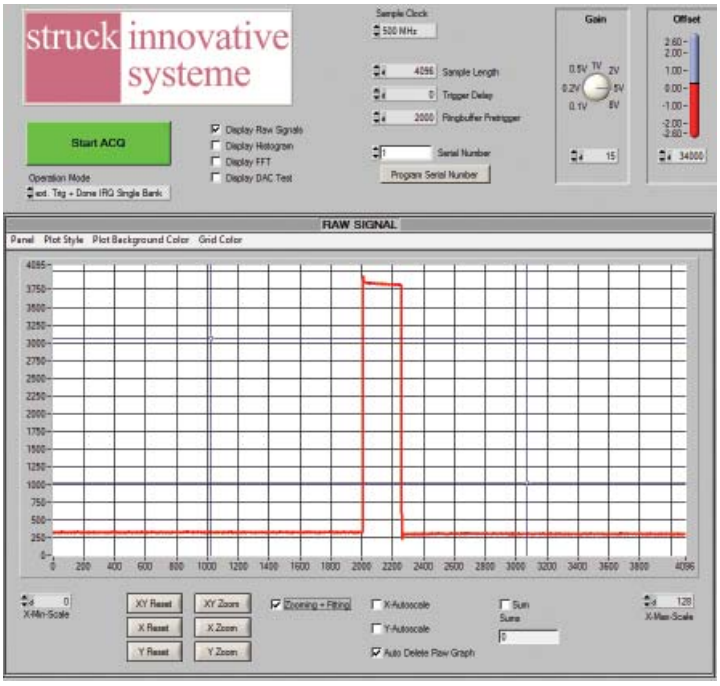
Functionality

- single Lane PCI Express PC add on card implementation
- one channel
- external TTL (SMA connector) and internal trigger
- 500 MS/s (10 MS/s - 500 MS/s)
- 2 x 64 KSamples/channel memory
- offset DAC
- VGA (variable gain amplifier)
- up to 250 MHz analog bandwidth
- ≤ +/- 6 V DC into 50 Ω SMA
- > 9 bit ENOB (@ 9.82Mhz sine FS)
- readout in parallel to acquisition
- dual bank mode
- XILINX Spartan 6 FPGA based
- in field JTAG and PCI EXpress firmware upgrade capability

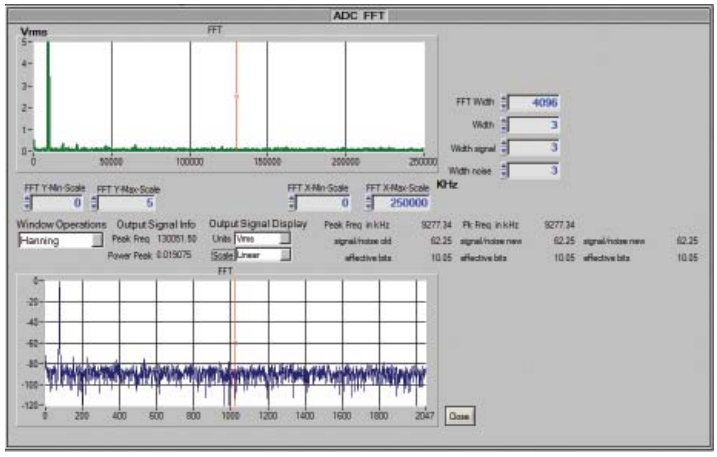
Software Support

- Windows 7 Driver API
- ready to run Labwindows CVI GUI
- more on request

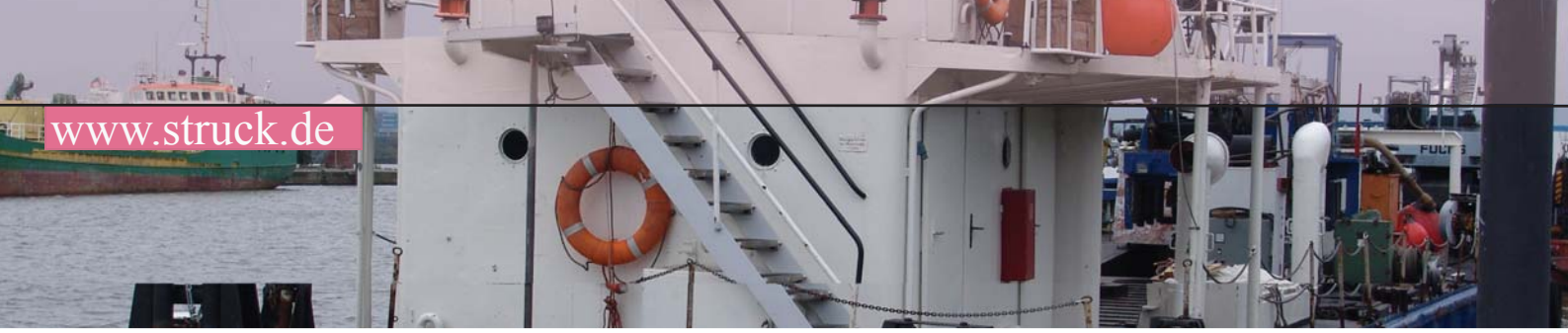
SIS1350 Digitizer



Screenshot of SIS1350 GUI



FFT of 9.28 MHz Sine in SIS1350 GUI



MTCA.4 (µTCA for Physics)

SIS8300 10 channel 16-bit 125 MS/s MTCA.4 Digitizer

ATCA and it's substandards like µTCA play an increasingly important role in the embedded world. The efforts of the PICMG workgroup xTCA for Physics to optimize the standard for next generation accelerators and experiments have resulted in the newly adopted MTCA.4 standard. The SIS8300 digitizer -developed for applications at the European XFEL e.g.- can be regarded as a demonstrator for the new standard.

Functionality

- 4 lane PCI Express connectivity
- 10 channels 125 MS/s 16-bit ADC
- 10 MS/s to 125 MS/s per channel sampling speed
- XC5VLX50T/XC5VSX50T-3FFG1136C Xilinx
- 25 MSample buffer memory per channel
- AC and DC input stage
- ADC inputs through Rear Transition Module (RTM)
- internal, front panel, RTM and backplane clock sources
- two 16-bit DACs for fast feedback implementation
- high precision clock distribution circuitry
- programmable delay of dual channel digitizer groups
- Gigabit link port implementation to backplane
- twin SFP card cage for high speed system interconnects

SIS8300 MTCA.4 Digitizer

Related xTCA Products	Page
SIS8100/3104 µTCA to VME Interface	5
SIS8100 µTCA FMC Carrier	24
SIS8100 µTCA Gigabit Link Card	24
SIS8900 RTM for SIS8300	22

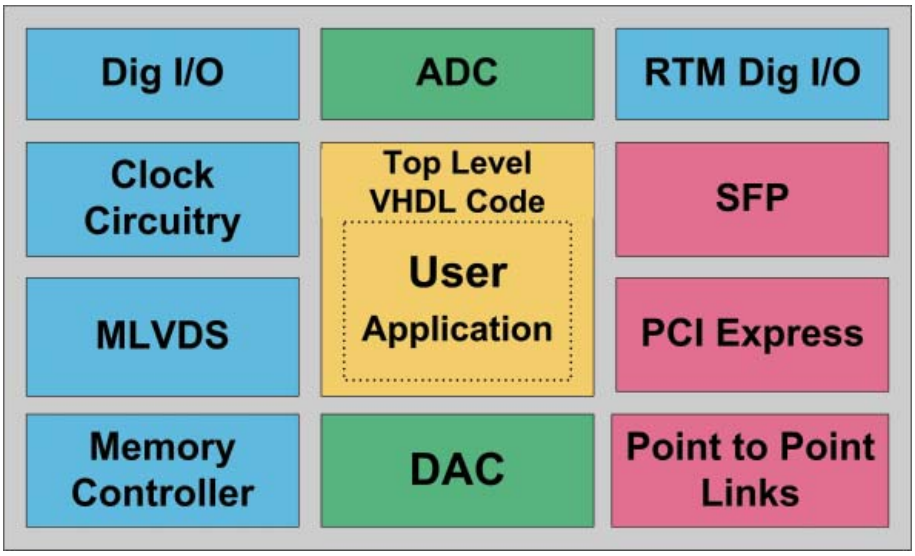
Name	Source	Description
SIS8900	Struck	Single Ended Input Card
RTM7201	HYTEC	4-channel Signal Modulator
DWC8300	DESY	Downconverter
BPM	DESY	Interleaved Sampling for BPM readout
APD	DESY	Dual Channel Signal Stretcher
Fast ADC RTM	SLAC	LLRF ADC Frontend

Available RTMs for SIS8300

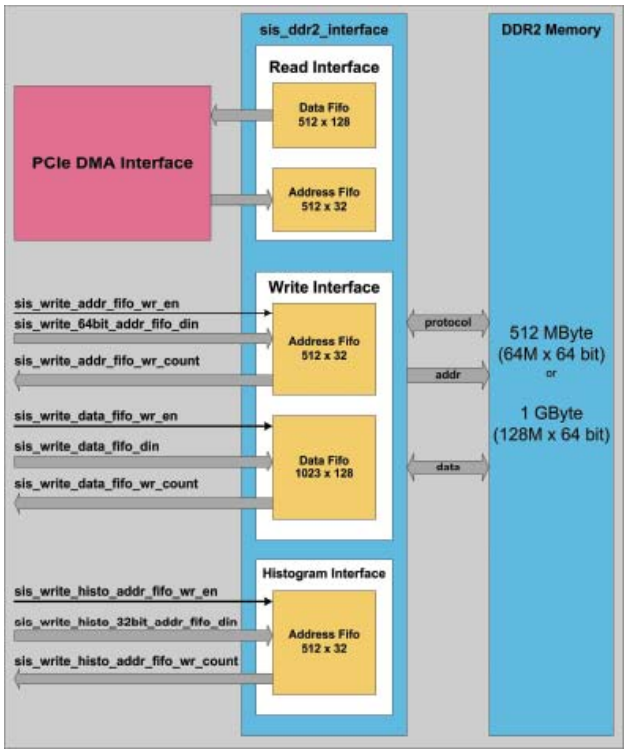
Development in co-operation with DESY
under ZIM Förderkennzeichen 2460101MS9

SIS8300 Firmware Aspects

The SIS8300 MTCA.4 digitizer was developed in co-operation with DESY for a variety of different applications at XFEL and demonstrator setups. A modular firmware approach allows for customization targeting the requirements of the specific application. An overview of the firmware building blocks is given in the diagram below.



SIS8300 Firmware Building Blocks



SIS8300 Memory Controller Block

DDR2 Memory Controller

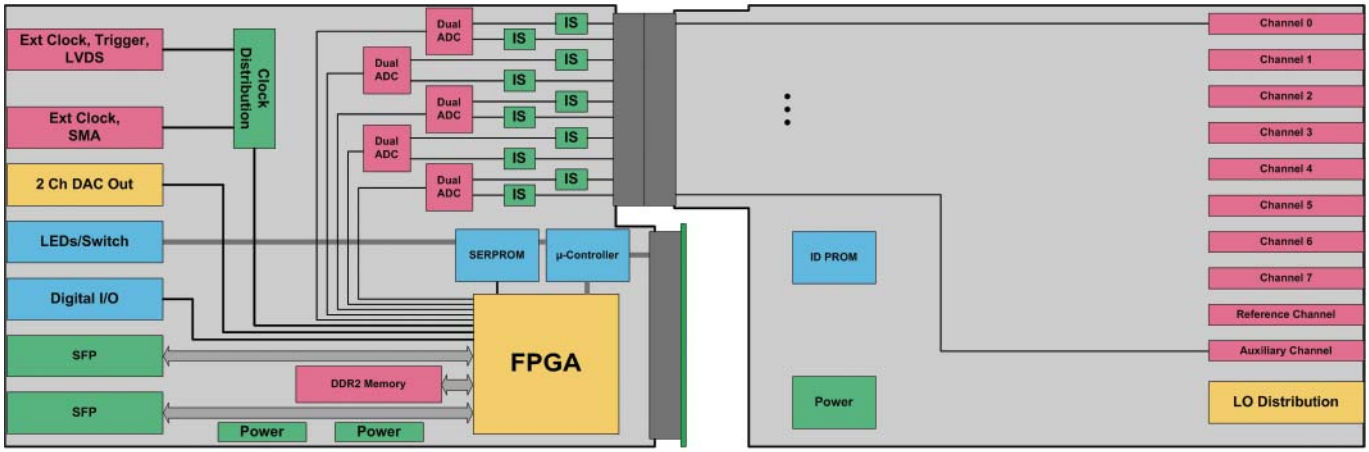
The memory controller block supports the 512 Mbyte and the 1 GByte memory options of the SIS8300. It interfaces to the 4-lane PCI Express with a read/write DMA interface. The histogramming memory controller supports an update rate of 5 MHz (20 MHz within one memory page amid differing three lowest order bits).

Full Custom Firmware

Feel free to inquire about a full custom firmware design development or customized application firmware for the SIS8300 digitizer to meet the requirements for your application.
The UCF file and required information about on board peripherals is provided to those who would like to develop their own full custom firmware design for the card in house.

SIS8300/Rear Transition Module Concept

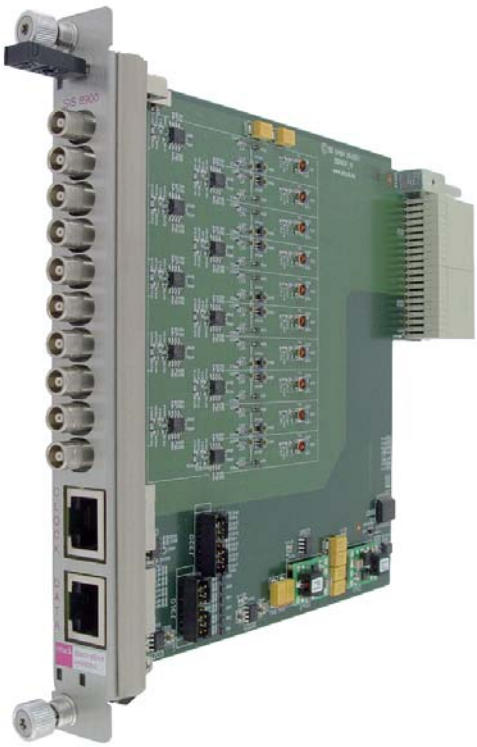
The µTCA for Physics Rear Transition Module (RTM) concept is illustrated below. It allows to use the SIS8300 digitizer with a variety of transition boards. Functionality like filtering or down-conversion can be offloaded from an external crate or on board design in a flexible fashion.



new

SIS8900 MTCA.4 Single Ended Input RTM for SIS8300 Digitizer

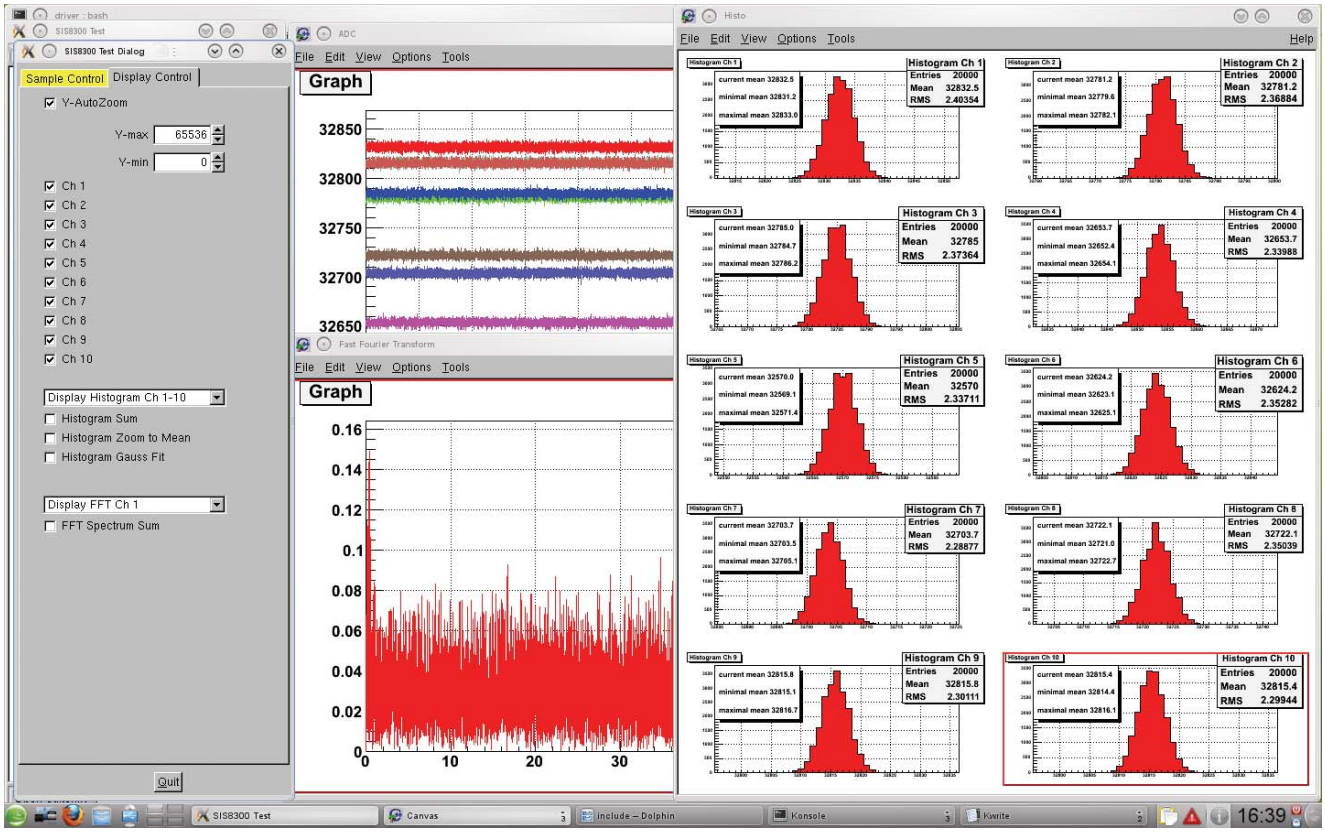
The SIS8900 RTM is used to feed single ended -50 Ω terminated- signals to the SIS8300 digitizer. Access to RTM _ CLK0, RTM_CLK1 and RTM_CLK2 and a couple of digital I/O lines is implemented in addition.



Functionality

- MTCA.4 (µTCA for Physics) RTM implementation
- 8-Bit I/O expander for I²C-bus
- 10 LEMO 00 connectors (FMB option)
- 50 Ohm input impedance
- -1 V,...,+1 V default input range
- analog signals can be routed to AC and DC input stage
- RJ45 jack for RTM clocks
- RJ45 jack for Digital I/O
- +5V, 250 mA power option for RJ45 jacks
- two metric on board pin headers for 6 LVDS input/output signals each

SIS8900 RTM



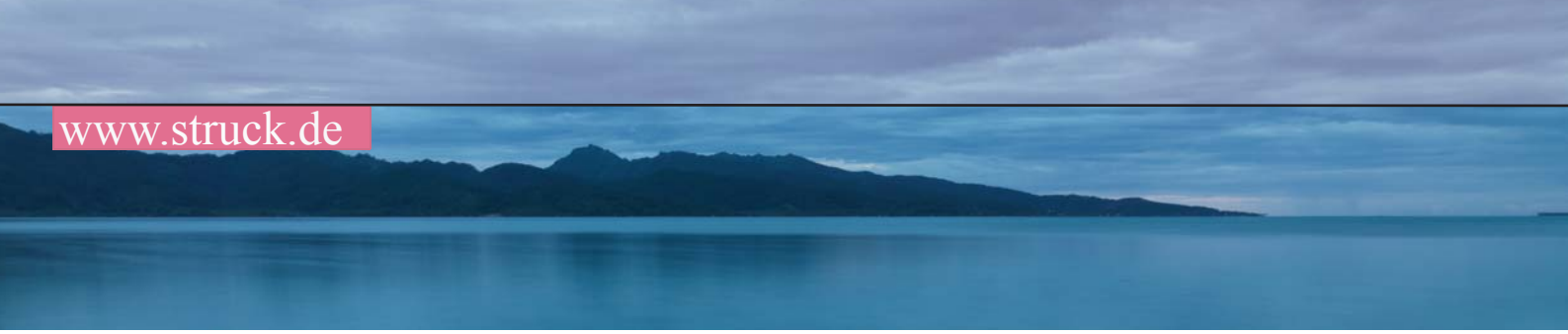
Screen Shot of SIS8300 ROOT GUI (under LINUX)

MTCA.4 / µTCA / SimpleTCA Systems

MTCA.4 (µTCA for Physics) System with CPU, Disk, Digitizers and MCH

The fairly young xTCA standards are adopted by more and more labs and universities around the world. In many cases the preference is on µTCA, the evolving µTCA for Physics and to some extend Simple µTCA We offer turnkey systems with components from different manufacturers as well as system integration and custom designs. The supported operating systems are Windows XP, Windows 7 and LINUX.

SimpleTCA System with CPU, Disk, I/O and Interface



µTCA/AdvancedMC

SIS8100 AMC GBit Link Card/VITA 57 FMC Carrier

The SIS8100 is a single width/mid-height AdvancedMC module with single lane PCI Express functionality (AMC.1). The first function is to extend our optical Link family into the xTCA world. The second stuffing option is the single VITA 57 FMC carrier, with target applications like fast I/O.

SIS8100 In Gigabit Link Configuration

Functionality

- AMC.1 AdvancedMC
- single width/mid-height
- PEX8311 PCI Express to local bus bridge chip
- Atmega128 based management
- Xilinx FX20 Virtex 4
- 1/2/4 GBit/s SFF link medium option or
- single FMC carrier option

Applications

- SIS8100/3104 µTCA to VME interface
- frontend data stream receiver
- digital I/O with FMC mezzanine
- analog I/O with FMC mezzanine

Software Support

- Windows 2K/XP/Vista/7
- LINUX Kernel 2.6
- NI Labview/Labwindows
- VisualC++

photographs: struck
front page XFEL cavity illustration
courtesy of DESY

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