

*Developments in xTCA for the SLAC National Accelerator Laboratory**

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Accelerator Requirements

Economical sparse low BW to dense high BW, throughput applications. Precise synchronization clock, timing, triggering extensions High availability redundancy options Rear Transition IO Cable Entry Hot Swap capable Economical Scalable from sparse to dense packaging COTS available

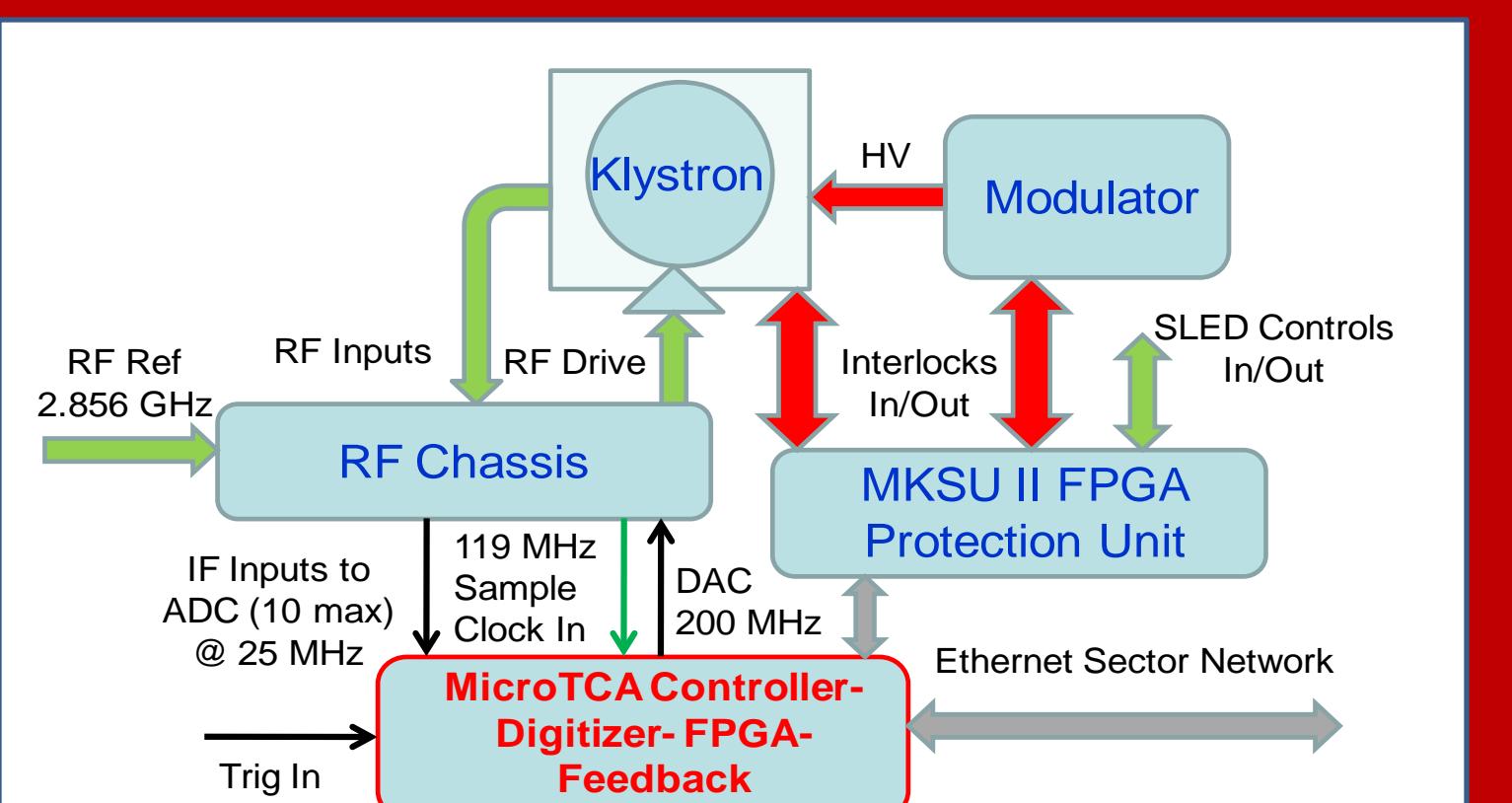
Detector System Requirements

Standard form factor, RTM interface MP Processor apps High power, cooling options Precise synchronization clock, timing distribution via extended options region Scalable range form factors, adapters Radiation resistant electronics, power converters for buried applications

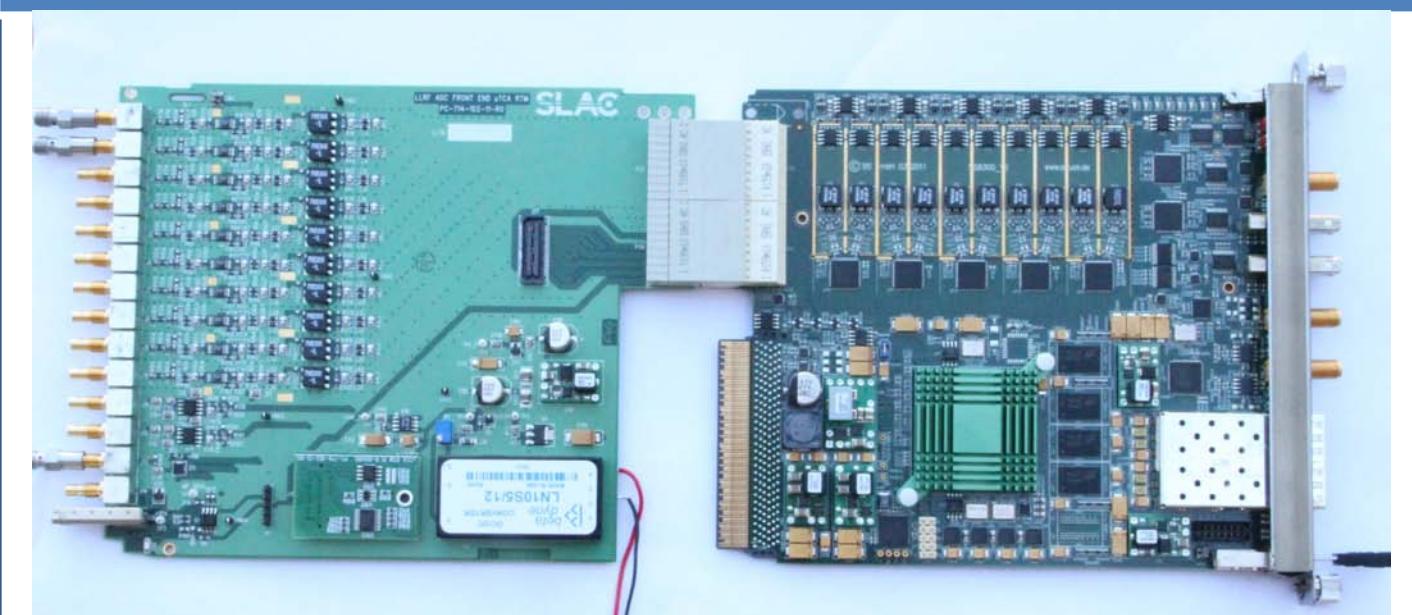
Generic AMC – Custom RTM Concept

MTCA.4 opens options for single-design AMC modules to be leveraged to many applications
Generic AMC examples:: Fast ADC-DAC multichannel AMC, RF, BPM, Toroid RTM for signal conditioning, calibration FPGA AMC Processor for RF Interlock, Photodiode, Camera RTMs
Industry Pack Adapter AMC to IO protection RTM for slow control, monitoring PMC AMC Adapter to interface RTM, many applications

Machine RF Phase Control to Femtosec Stability FPGA Based



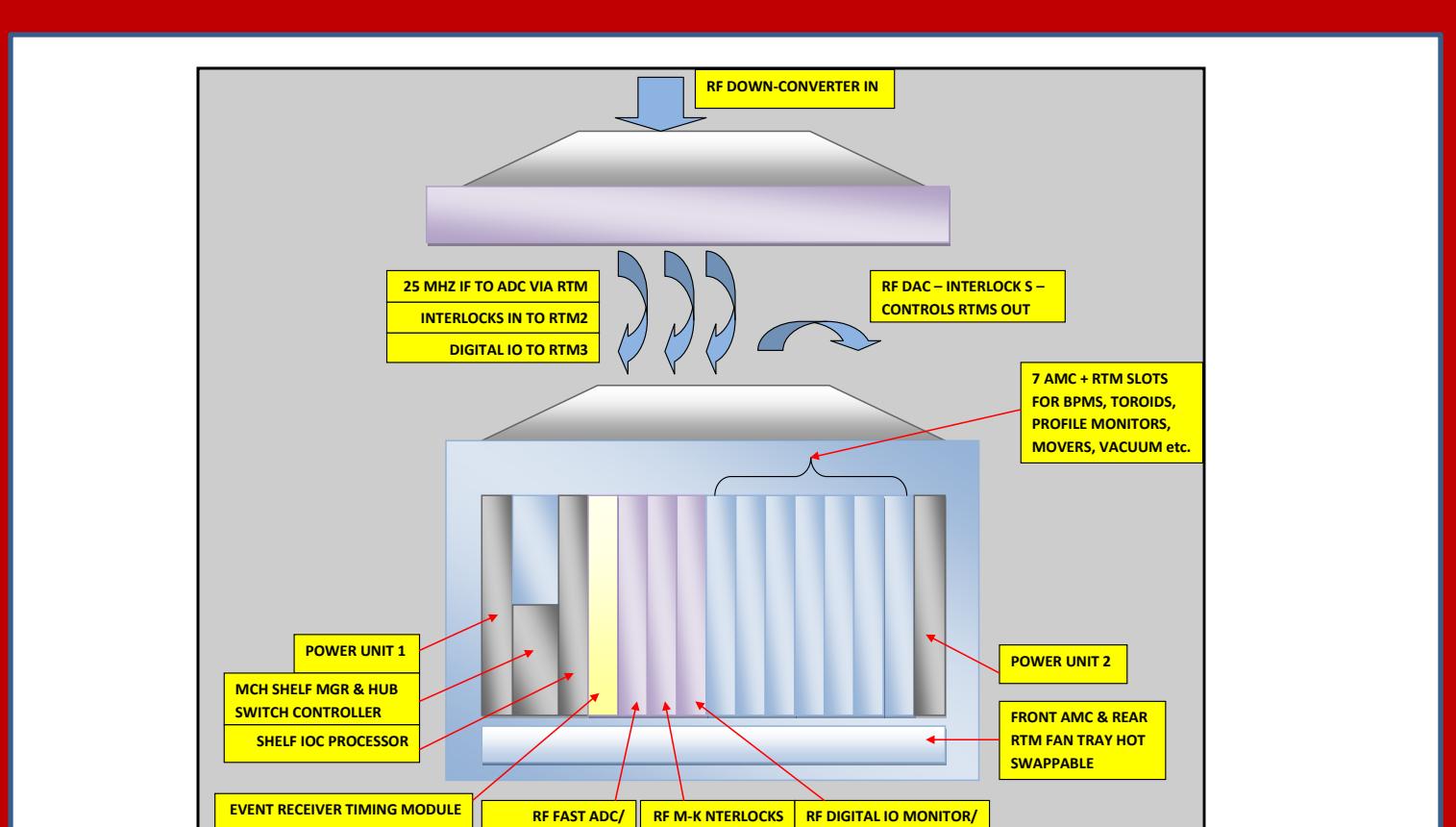
RF Power System w/ MTCA.4 Shelf



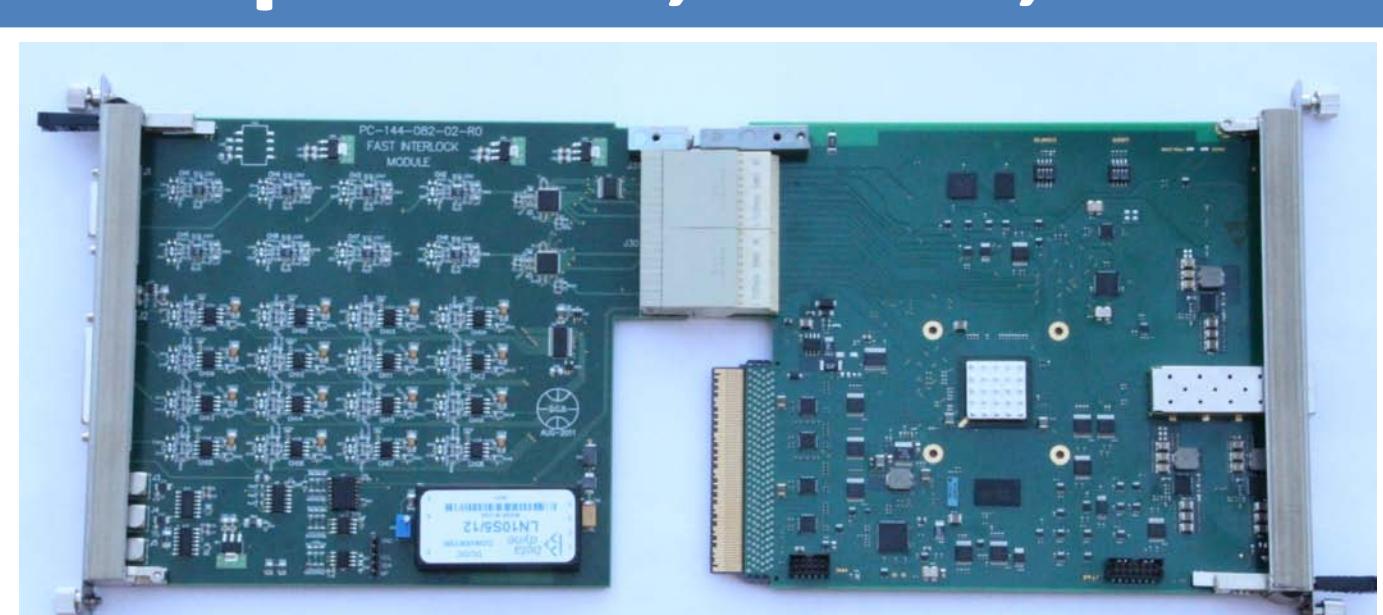
RTM Interface (SLAC) ADC-DAC (Struck)

Courtesy A. Young, Z. Geng, SLAC & Struck Co.

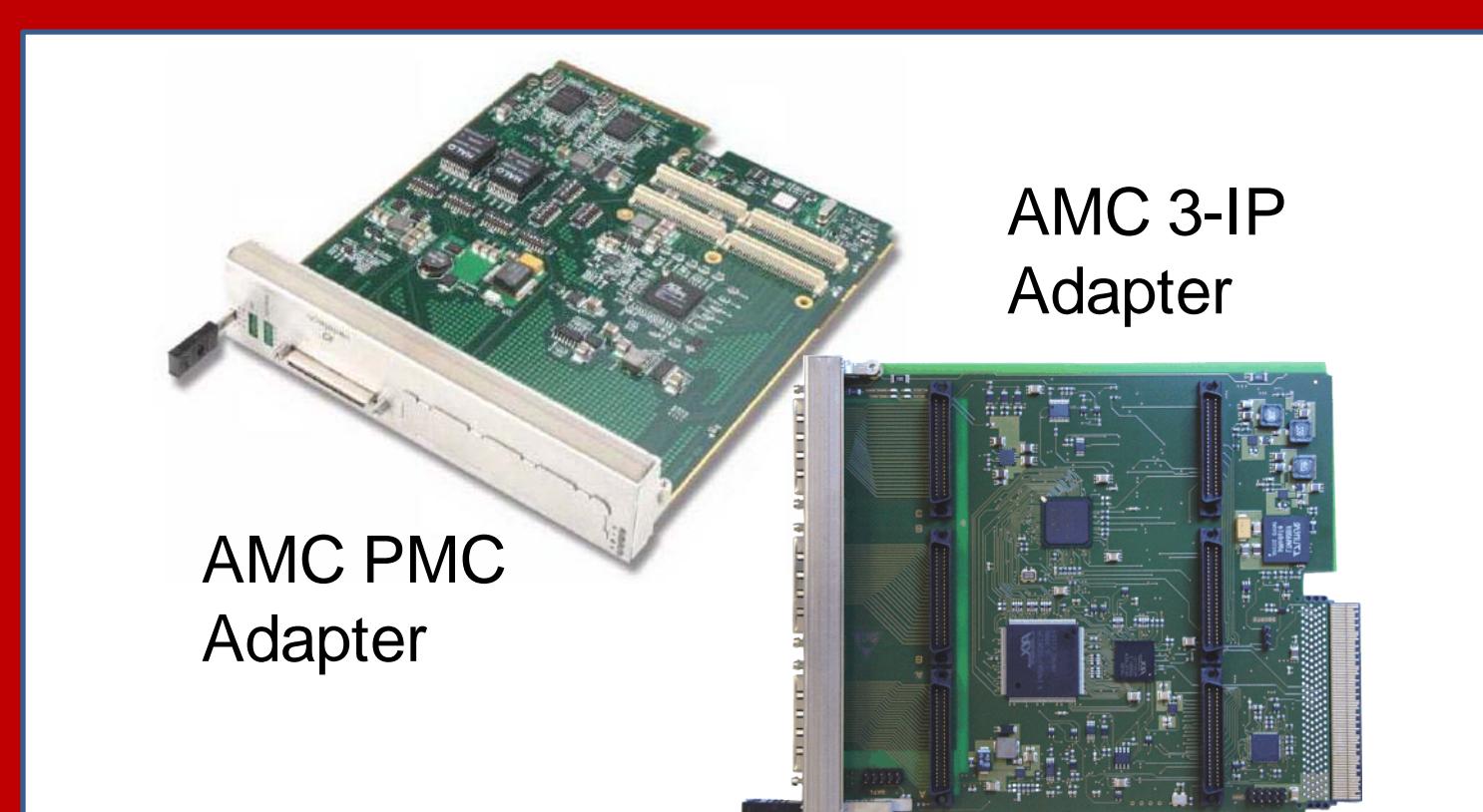
RF Power System Interlocks FPGA Based



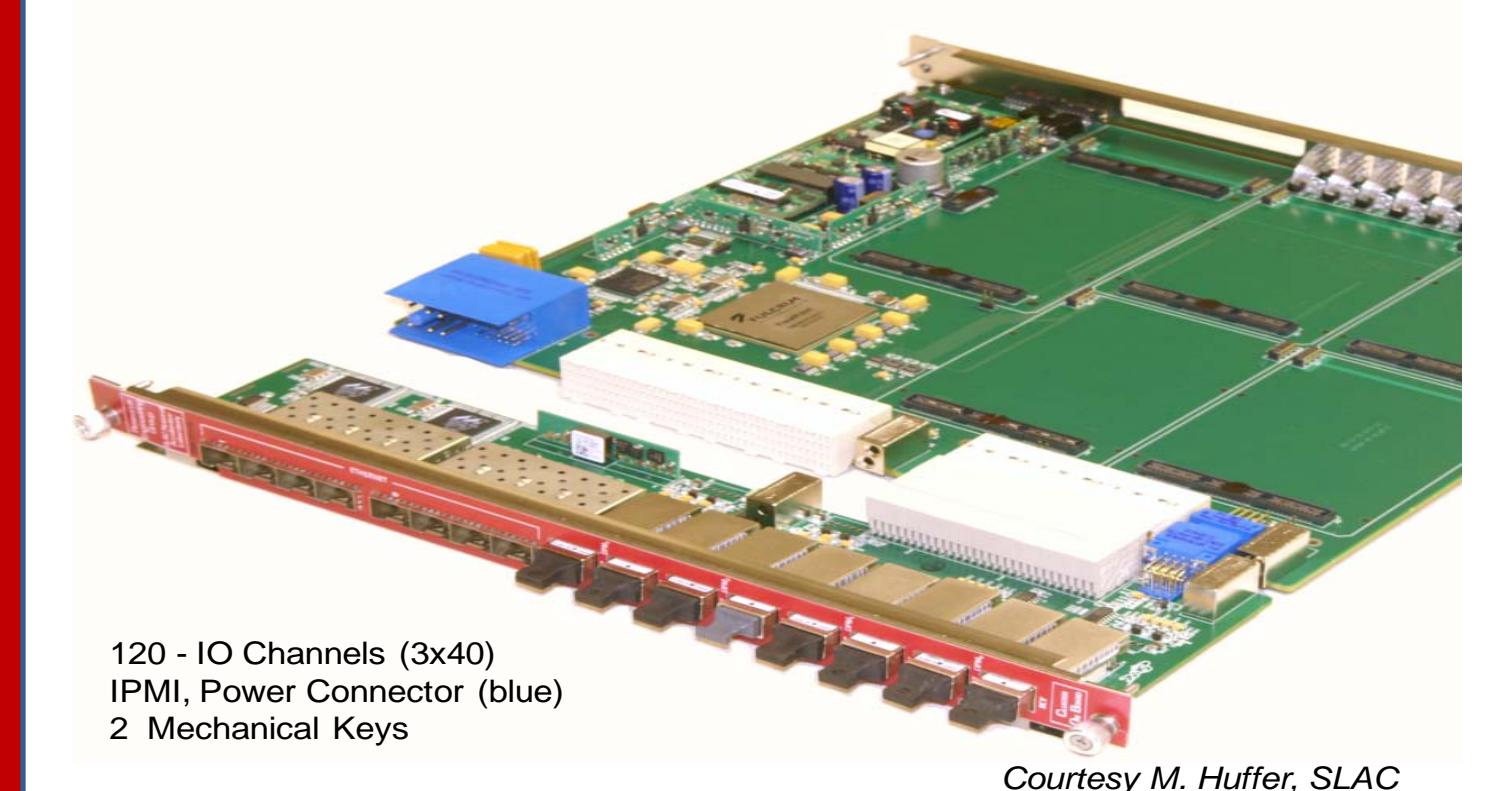
MTCA.4 Control Node Complete RF, Intlk, Cntrs



MTCA Adapters, ATCA Massively Parallel Processor



PMC, 3-IP Adapters* *MTCA.0 Versions



First PICMG3.8 Implementation (SLAC)

Courtesy Vadatech, TEWS, M.Huffer.

Courtesy D. Brown & TEWS Co.