VHDL Implementation of Feature-Extraction Algorithm for the PANDA Electromagnetic Calorimeter

M. Kavatsyuk, E. Guliyev, P.J.J. Lemmens, H. Löhner, *Member, IEEE*, G. Tambave
KVI, University of Groningen, Groningen, The Netherlands
on behalf of the PANDA Collaboration

***Abstract*—The feature-extraction algorithm, developed for the digital front-end electronics of the electromagnetic calorimeter of the PANDA detector at the future FAIR facility, is implemented in VHDL for a commercial 16 bit 100 MHz sampling ADC. The use of modified firmware with the running on-line data-processing algorithm will allow to perform realistic performance studies of the calorimeter and test a trigger-less readout concept of the data acquisition for the PANDA experiment.**

I. Introduction

The mass of the proton and, therefore, of the visible Universe, originates from the strong interaction among the three elementary light quarks confined in the proton, but the exact mechanism of the underlying dynamics is yet unknown. Charm-meson resonances and yet undiscovered glueballs might reveal the origin of the hadronic mass spectrum. The PANDA collaboration at the future FAIR synchrotron facility at Darmstadt, Germany, will employ antiproton annihilations to investigate resonances in the charmonium mass region.

The Electromagnetic Calorimeter (EMC) [1] of the PANDA detector comprises of the central target calorimeter, read out by large-area avalanche photodiodes (LAAPD), and the forward endcap EMC, read out by vacuum phototriodes (VPT). Cooled $PbWO_4$ (PWO) scintillating crystals will be employed for the detection of high-energy photons, electrons and neutral mesons. The barrel EMC will be placed inside the 2 T solenoid magnet of the target spectrometer. The gain of the selected photo-sensors is not sufficient to directly digitize the output signals. Therefore, special low-power and low-noise preamplifiers were developed. The discrete component preamplifier (LNP) [2] will be used for the VPT readout, and the ASIC APFEL-II [3] for the LAAPD readout. The ASIC has a built-in two-stage shaper and provides two output signals with high and low gains. The discrete preamplifier is a one-range resistor-reset type with decay constant of 25 μs. The signal shapes provided by the ASIC and the discrete preamplifiers are shown in figure 1.

The PANDA experiment will make use of an antiproton beam on a frozen hydrogen-pellet target. Therefore, we expect a strong angular dependence of the event-rate distribution in the EMC and, due to pellet density and frequency fluctuations, also event-by-event fluctuations. Event rates of 10 kHz are expected in the barrel part of the EMC, with rates up to 150 kHz in the most forward region. The forward endcap EMC will be exposed to event rates up to 750 kHz. Due to these rate variations, different photo-sensors and preamplifiers will be employed for different parts of the EMC. For optimal conditions of event selection the PANDA experiment will use a trigger-less data acquisition system. Each sub-detector will continuously provide all single-hit event information. Therefore, the EMC-preamplifier signals will be continuously digitized by sampling ADCs (SADC) and the data will be processed on-line in FPGAs.

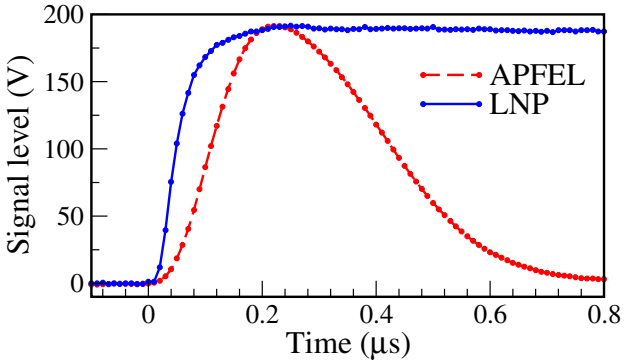

Fig. 1. The pulse shapes measured for the discrete preamplifier (blue solid line) and for the ASIC APFEL-II with high gain output (red dashed line).

The aim of the investigations presented here is to implement in VHDL and test a simple, efficient, and robust feature-extraction algorithm, described in ref. [4], to perform the on-line signal-trace processing.

II. Materials and Methods

The implementation of the feature-extraction algorithm [4] is done using portable VHDL and is tested on a Xilinx Spartan 3 FPGA. To test the implementation and the performance of the algorithm a series of measurements with the PANDA-EMC prototype was performed. The test set-up consisted of a single $(20 \times 20) \times 200$ mm^3 PWO scintillating crystal with LAAPD photo-sensors attached at both (20×20) mm^2 ends of the crystal. Both, LNP and APFEL preamplifiers were used to acquire data samples. The output signals were digitized by a 100 MHz 16 bit SIS3302 SADC [5]. For each event 10 μs long traces were stored for the off-line analysis. The obtained

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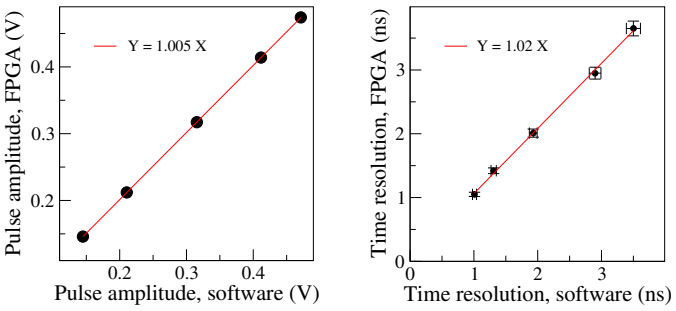

Fig. 2. The correlation of the measured pulse amplitude and the time resolution obtained by analysing the same data using the software and the hardware (FPGA) implementations of the feature-extraction algorithm.

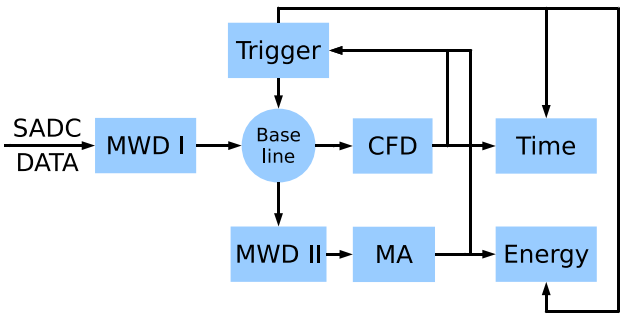

Fig. 3. Block-diagram of the feature-extraction algorithm implemented in VHDL.

data were analysed off-line using a PC and semi-online in the FPGA. The FPGA analysis was performed using a Xilinx Spartan 3A-N design board. The transfer of measured data to the FPGA board and the read-out of the extracted time and energy information were done using a serial RS232 interface. Figure 2 shows the comparison of the results obtained using the software and the hardware processing of the same data. The data, employed for the presented comparison, was measured using above described single-crystal set-up with the APFEL ASIC preamplifier. Correlation coefficients of about 99.8 % were determined. Similar results were obtained with the LNP preamplifier.

After verification of the VHDL implementation with the test data, the firmware was ported to the 100 MHz 16 bit SIS3302 SADC [5] module, which is used for the test experiments with the PANDA-EMC prototypes. The use of modified firmware with the running on-line feature-extraction algorithm will allow us to perform realistic performance studies of the calorimeter. Moreover, it will be possible to test a trigger-less readout concept of the data acquisition, namely to store information about all hits in all the channels of the calorimeter and identify cluster events using recorded time-stamps.

III. Feature-extraction algorithm

The block-diagram of the implemented feature-extraction algorithm is shown in figure 3. Depending on the type of the input signal it is possible to select different processing paths of the digitized data. For the LNP preamplifier, a resistor-reset charge-integrating preamplifier with the discharge time-constant of 25 μs, an additional digital pulse-shaping is

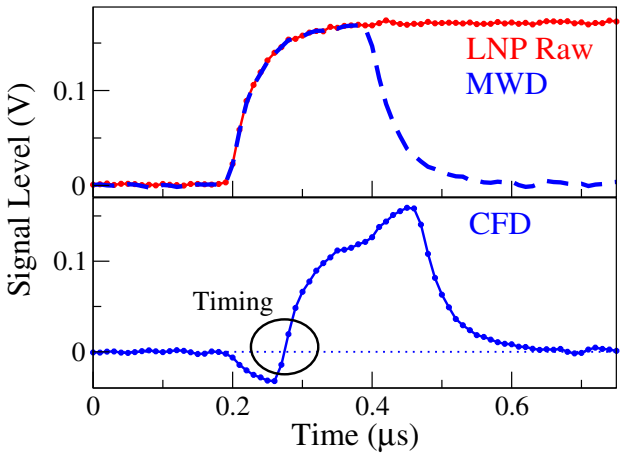

Fig. 4. The raw LNP signal and the resulting MWD pulses (upper panel, red solid and blue dashed lines, respectively) and the CFD signal (lower panel).

applied. The raw data from the SADC is processed using the Moving Window Deconvolution filter [6] (MWD). The effect of the MWD filter on a LNP pulse is shown in figure 4. The MWD allows to recover the exponential decay of the LNP signal and produces a step-like function which, after differentiation, results in a semi-rectangular shape of the required length. After the MWD shaping a constant signal-offset is removed by the base-line follower. The base-line is calculated as an average of a specified number of samples before the pulse. Data of the detected pulses are not taken for the base-line determination.

The base-line subtracted signal is used for triggering and time-stamp determination. The digital implementation of the constant-fraction discrimination (CFD) algorithm is applied to obtain precise timing information. The linear interpolation using two data-points, see figure 4, is employed for finding the zero-crossing point with a much higher precision than the sampling period. For the EMC prototype it was possible to achieve a time resolution better than 1 ns while using a 50 MHz sampling rate for the SADC.

The Moving Average filter (MA) is used to reduce high-frequency noise. The pulse-detection is done employing combined information from the CFD and MA filters. Once the zero-crossing transition is detected in the CFD signal the output of the MA filter is compared with a threshold. After the identification of the pulse the maximum value of the MA signal is taken as an amplitude measurement.

In case of a signal with finite rise-time, the MWD filtering provides a pulse with the required width, with non-distorted leading edge and the same length for trailing and leading edge, see figure 5. For the PANDA-EMC prototype equipped with the LNP preamplifiers we found that the raw signal has two components with different rise times. Therefore, to achieve the best energy resolution and lowest signal-detection threshold, it is necessary to use the MWD with a differentiation constant longer than 200 ns, as shown in figure 5. The shorter differentiation constant reduces the resulting pulse amplitude. This effect does not allow to get the optimal performance of the detector at high hit-rates as the long filtered pulses will pile

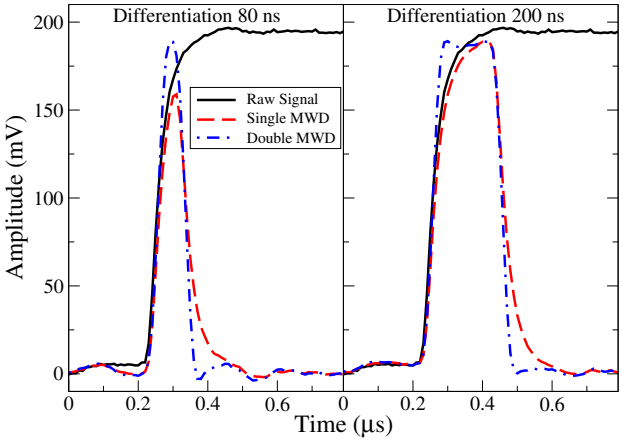

Fig. 5. The pulse shape measured for the EMC prototype with LNP preamplifier (black solid line) and resulting pulses after single (red dashed line) and double (blue dash-dotted line) MWD filtering.

up and such events will be lost. However, the use of the second MWD filter allows to overcome this limitation. As can be seen in figure 5, the second MWD filter restores the original pulse amplitude even at shorter MWD differentiation constants at the cost of distortion of the rising edge of the pulse. Therefore, to use all advantages of a double MWD filtering the second MWD filter is employed only in the triggering and energy-readout chain, see figure 3.

The above described feature-extraction algorithm is used in case of an unshaped input signal. If an analogue shaping is employed, like in case of the APFEL ASIC preamplifier (see figure 1), both MWD filters of the signal-processing algorithm are not needed and, therefore, can be bypassed.

IV. VHDL IMPLEMETATION

The used SIS3302 VME module [5] is a 8-channel 16 bit 100 MHz sampling ADC. Data from SADC chips are fed to FPGAs for processing. For every two input channels one Xilinx Spartan XC3s1000-5 FPGA is available. The incoming data from the SADC chips are 16 bit wide and of unsigned-integer type. For processing with the feature-extraction algorithm this data are converted into 17 bit signed format and all further calculations are done with this precision.

The MWD I and II filters, see figure 3, have two parameters, namely the length and the correction constant. Both of these parameters can be changed by programming corresponding registers of the SADC module. In order to save FPGA resources, the MWD-length parameter can take values which are powers of two: 2, 4, 8, 16, 32, 64. This selection of the MWD length simplifies the implementation of the division, one of the internal operations required by the filter. Both MWD filters in the feature-extraction algorithm can be bypassed by setting register values. Such a possibility allows to use the same firmware for the shaped and non-shaped signals.

The base-line follower determines and removes the constant offset of the incoming signal. To determine the base-line an average of 512 data-samples before the pulse is used. Once the pulse is detected, the base-line averaging is deactivated for the whole duration of the pulse. The implementation of the base-line follower foresees continuous averaging, as described above. However, it is possible to force to perform the base-line initialisation only once. In this case, the same value is used over all the running period.

The constant-fraction pulse is derived from the shaped and base-line subtracted signal. The parameters of the CFD filter are a fraction value and a delay. The delay should be adjusted to match the rise time of the measured pulse. The maximum possible value of the CFD-delay register is 32 SADC samples, which corresponds to 320 ns at 100 MHz sampling rate. The fraction value can be set to either 1/2 or 1/4. For the time-stamping of the pulse the zero-crossing is detected. To achieve a sub-sample precision the successive interpolation between the two samples is used, below and above zero level. The interpolation is done with nine iterations yielding a precision of $T/2^9$, where T corresponds to the sampling period.

The energy readout is done after the MA smoothing, see figure 3. The length of the MA filter can be adjusted by setting the register values. After the pulse detection, the extracted energy and time values are written into the buffer memory. The available buffer may store up to 4 million detected events. Once the buffer is full, the new data will be replacing the oldest one. The acquisition can be stopped using either an external logic pulse, provided via the front panel of the module, or by sending a special ”stop” command via VME bus. Once the acquisition is stopped, it is possible to read the data from the buffer. The number of acquired events is provided by a dedicated register.

In addition to the described mode of operation, the firmware has a number of debugging options. Namely, it is possible to store the output of all filters directly into the buffer memory. This feature simplifies the procedure of optimizing the filter parameters.

V. OUTLOOK

The aim of this project is to develop and implement in VHDL a simple, efficient, and robust feature-extraction algorithm for the front-end electronics of the PANDA EMC. The above described implementation of the algorithm is a first step towards building a complete trigger-less readout chain. While the dedicated digitizer modules for the PANDA EMC are being developed, the SIS3302 VME SADC was selected to perform test measurements with different detector prototypes. The modified firmware of the SADC allows to process on-line digitized wave forms and to store only the energy and time information of the detected hits. This data is transferred to the PC, where the search for hit correlations takes place. Simultaneous hits in different channels are combined into events.

The current version of the feature-extraction algorithm is very flexible in terms of parameter selections. This allows to achieve the best performance with different types of signal sources. Therefore, this development might be of interest for other experiments. For the PANDA EMC the aim is to find the best combination of the parameters. With the current design of the firmware it is possible to process data for 16 channels with

the second smallest Xilinx Virtex6 FPGA, leaving room for the implementation of data-transfer protocols. For the final design of the feature-extraction algorithm most of the parameters will be hard-coded in the firmware, therefore, even more reducing resource requirements. In addition to the described functionality, a pile-up detection and recovery algorithm will be implemented to improve the performance of the detector at high counting rates.

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